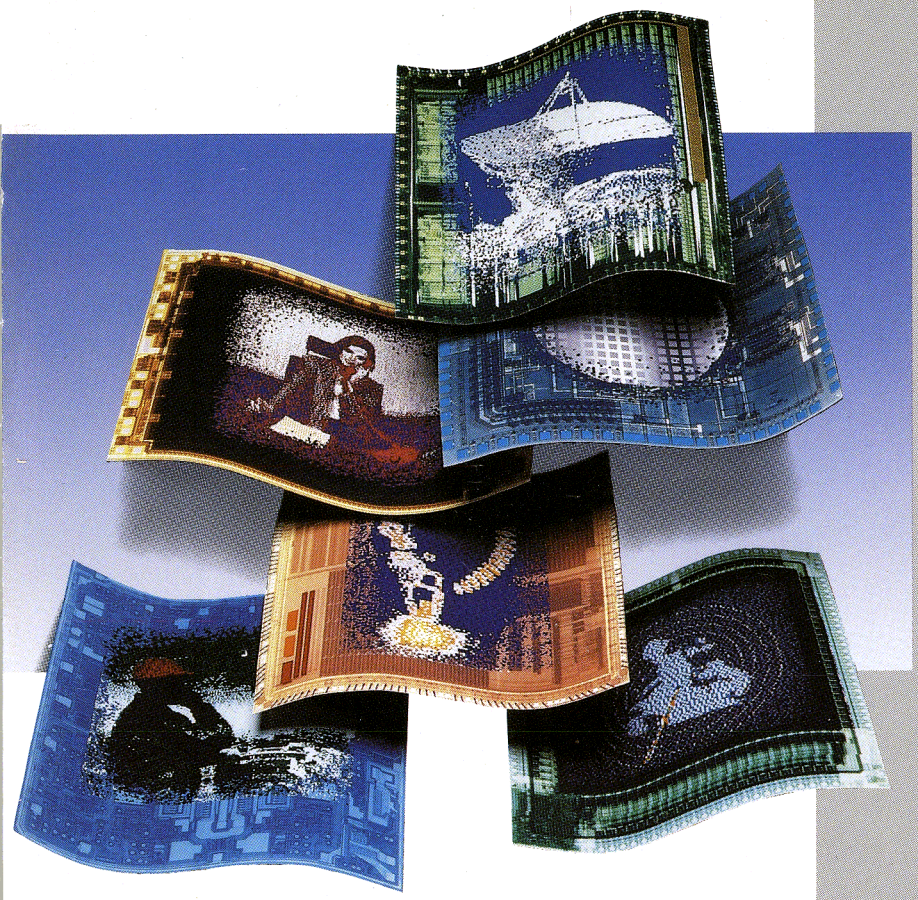
Personal Communications

May 1992

IC Handbook



GEC PLESSEY
SEMICONDUCTORS

PERSONAL COMMUNICATIONS

IC Handbook

Foreword

GEC Plessey Semiconductors are leaders in the growing market of Personal Communications.

The features which identify ICs as being suitable for this market area are *supply current* and *frequency*. Since battery life is all-important in hand-held equipment, every effort is made by our IC designers to develop products which require the absolute minimum current. New ICs such as the SL6639 pager chip and SP8705 (a programmable multi-modulus divider, which consumes only 5mA at 1100MHz) exemplify this philosophy.

New frequency band allocations have been made in the 450 and 900MHz regions for pagers, cordless telephones and cellular radios. GPS bipolar processes have been developed to operate at these and even higher frequencies for dividers, IF amplifiers and single chip synthesisers. The 1 Micron CMOS process is also capable of operating at high frequencies and the latest generation of CMOS synthesisers are included in this handbook.

All the relevant GPS ICs can be supplied in surface mount miniature plastic and some in plastic quad packages in order to satisfy the requirement for small size in compact hand-held radio equipment.

Finally, the Quality Assurance Procedures that are applied to GEC Plessey Semiconductors' products (from consumer electronics to defence projects) are applied to Personal Communications ICs with rigour. Performance and long term reliability are thereby guaranteed in what can be demanding operating enviroment.

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* Outline or development details only - contact GPS Customer Services (see page 263)

** For maintenance purposes only

Product List - alpha numeric

* Outline or development details only - contact GPS Customer Services (see page 263)

** For maintenance purposes only

Technical Data

GEC PLESSEY
SEMICONDUCTORS

DS 3307- 1

MV3100

3V CODEC WITH ANALOG INTERFACE FOR DIGITAL MOBILE TELEPHONES

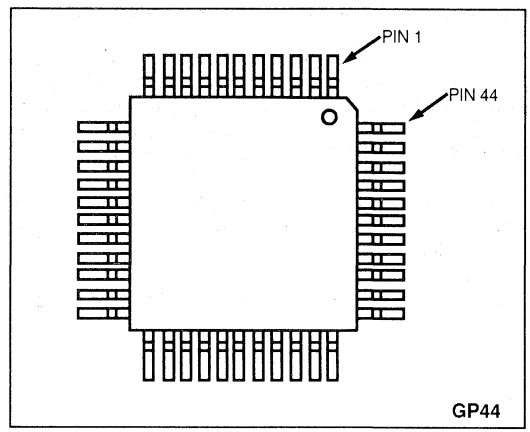
The MV3100 is a complete integrated audio interface for digital mobile telephones. Using mixed signal CMOS technology the device contains a DSP CODEC for audio to PCM conversion, together with gain programmable microphone and loudspeaker amplifiers. The use of DSP architecture for the CODEC function enables device operation from supplies of 2.7V upwards and allows software programmability of gain characteristics. The device requires a minimum of external components giving a physically small solution, ideal for hand-portable telephones.

FEATURES

- Highly integrated solution with on-chip audio interface
- Low voltage operation, 2.7V to 5.5V
- Low power consumption, 32mW typ.
- Excellent RF immunity
- 16Bit linear PCM interface
- Gain programmability supports many microphone and loudspeaker types
- On-chip PLL generates all internal clocks
- Programmable sidetone

APPLICATIONS

- Digital Cordless Telephones (CT2, DECT, JDCT, Spread Spectrum)
- Digital Cellular Telephones (GSM, ADC, JDC)
- Digital Mobile Radio



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.3V to +7V
Input Voltage	-0.3V to V_{DD} +0.3V
Operating Temperature	-30°C to +70°C
Storage Temperature	-55°C to +125°C

MV6639

POCSAG DECODER

The MV6639 POCSAG decoder is capable of operating at 512 or 1200 baud. This device together with a suitable receiver provide the major components for a POCSAG pager.

POCSAG is the acronym for Post Office Code Standardisation Advisory Group. The POCSAG code is the most accepted radio paging standard, (CCIR RPC No.1) and provides for over 2 million pager ID's, two of which may be held in this device. The POCSAG code format is shown in figure 3.

The design is optimised for very low power, low voltage use. Advanced features allow the decoder to be used in a wide range of applications.

The pinout and architecture are shown in figures 1 and 2

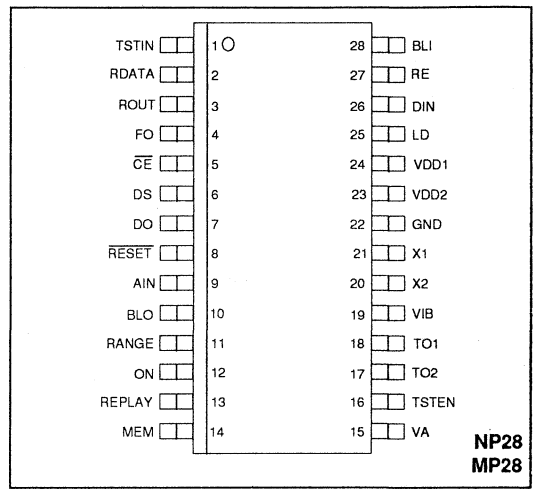


Fig. 1 Pin connection
(top view - not to scale)

FEATURES

- Tone only and/or messaging pager at 512 or 1200 baud using a single 32768Hz crystal
- Low voltage supply (1 V min.)
- Low current consumption (100µA max.)
- Interface to SL6649- 1 radio receiver chip
- True 2 bit CRC error correction
- Voltage doubler for radio receiver or µP and Display
- Programmable tone generator output frequency (2048 or 2731 Hz)

APPLICATIONS

- Wrist watch pager
- Message display pager
- Tone only pager
- Data receivers

ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD1 - GND)	-0.5V to 5V
Voltage on any pin	-0.3V to VDD1 + 0.3V
Operating temperature	-20°C to + 70°C
Storage temperature	-55°C to +125°C

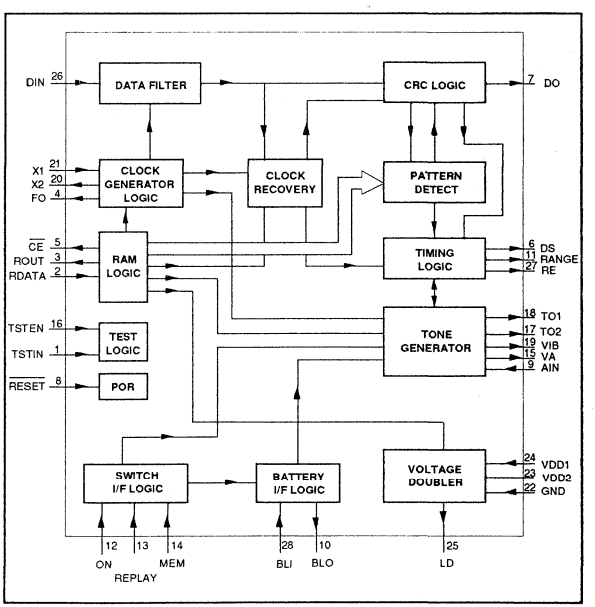


Fig. 2 MV6639 Block Diagram

DS3277-1.2

NJ8820

FREQUENCY SYNTHESISER (PROM INTERFACE)

The NJ8820 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words read from an external memory, with the necessary timing signals generated internally.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8820 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of −30°C to +70°C. The NJ8820MA is available only in Ceramic DIL package with operating temperature range of −40°C to +85°C.

FEATURES

- Low Power Consumption
- Direct Interface to ROM or PROM
- High Performance Sample and Hold Phase Detector
- >10MHz Input Frequency

ORDERING INFORMATION

NJ8820 BA DP Plastic DIL Package
NJ8820 BA MP Miniature Plastic DIL Package
NJ8820 MA DG Ceramic DIL Package

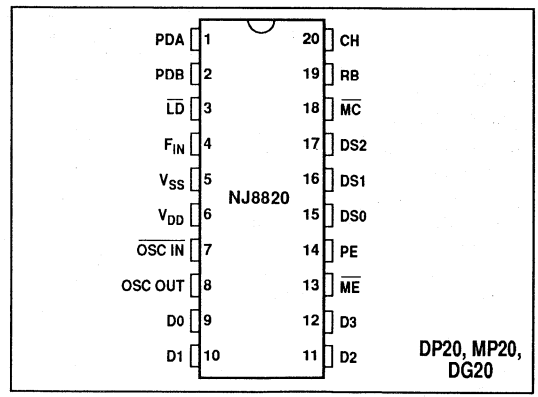


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}-V_{SS}$	−0·5V to 7V
Input voltage	
Open drain outputs, pins 3 and 13	7V
All other pins	V_{SS}−0·3V to V_{DD}+0·3V
Storage temperature	−65°C to +150°C (DG package, NJ8820MA)
Storage temperature	−55°C to +125°C (DP and MP packages, NJ8820)

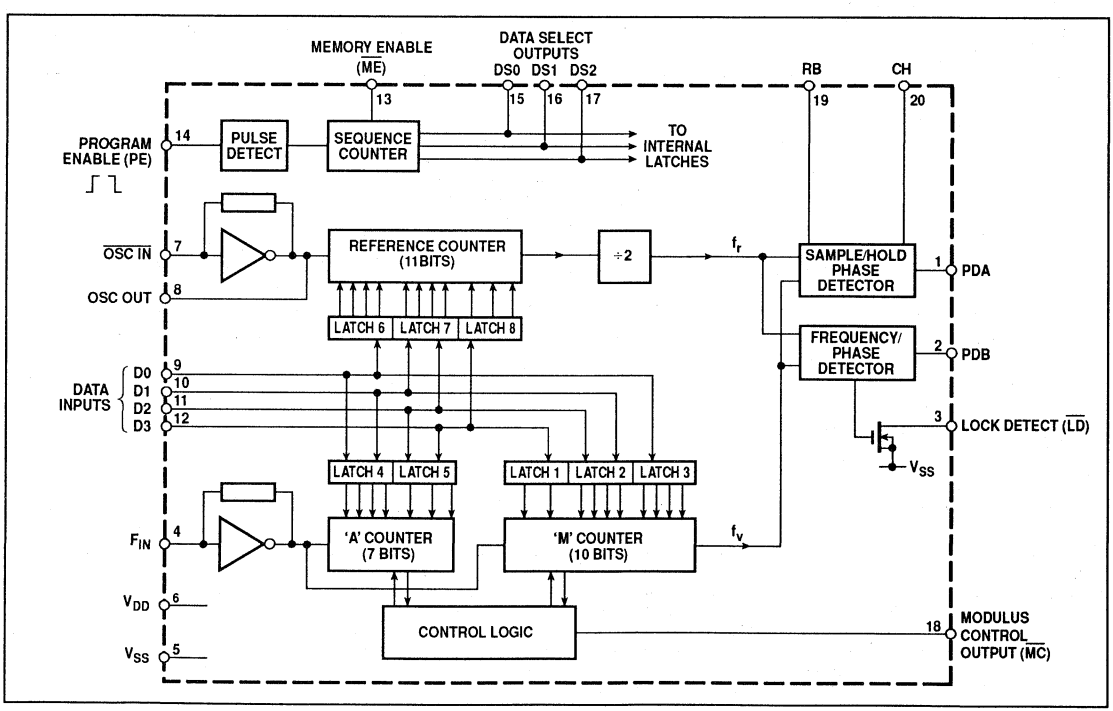


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS AT V_{DD} = 5V

Test conditions unless otherwise stated:

V_{DD}–V_{SS}=5V ±0·5V. Temperature range NJ8820 BA: –30°C to +70°C; NJ8820 MA: –40°C to +85°C

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3·5	5·5	mA	f_{osc}, f_{FIN} = 10MHz } 0 to 5V square wave
		0·7	1·5	mA	f_{osc}, f_{FIN} = 1·0MHz }
OUTPUT LEVELS					
Memory Enable Output ($\overline{ME}$)					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7	V	
Data Select Outputs (DS0-DS2)					
High level	4·6			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 2mA
Modulus Control Output ($\overline{MC}$)					
High level	4·6			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 1mA
Lock Detect Output ($\overline{LD}$)					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7	V	
PDB Output					
High level	4·6			V	I_{SOURCE} = 5mA
Low level			0·4	V	I_{SINK} = 5mA
3-state leakage current			±0·1	µA	
INPUT LEVELS					
Data Inputs (D0-D3)					
High level	4·25			V	TTL compatible
Low level			0·75	V	See note 1
Program Enable Input (PE)					
Trigger level	V_{BIAS} ±100mV			V	V_{BIAS} = self-bias point of PE (nominally V_{DD}/2)

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
F_{IN} and $\overline{OSC\ IN}$ input level	200			mVRMS	10MHz AC-coupled sinewave
Max. operating frequency, f_{FIN} and f_{osc}	10·6			MHz	Input squarewave V_{DD} to V_{SS}, See note 5.
Propagation delay, clock to $\overline{MC}$		30	50	ns	See note 2.
PE pulse length, t_W	5			µs	Pulse to V_{SS} or V_{DD}.
Data set-up time, t_{DS}	1			µs	
Data hold time, t_{DH}	10			ns	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	See note 3.
Output resistance, PDA			5	kΩ	
Digital phase detector gain		0·4		V/Rad	
Power supply rise time	100			µs	10% to 90%, see note 4.

NOTES

1. Data inputs have internal pull-up resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5µs, typically.
4. To ensure correct operation of power-on programming.
5. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESCRIPTIONS

Pin no.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at $(V_{DD}-V_{SS})/2$ when the system is in lock. Voltage increases as f_V phase lead increases; voltage decreases as f_r phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB).
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_V > f_r$ or f_V leading: positive pulses with respect to the bias point V_{BIAS} $f_V < f_r$ or f_r leading: negative pulses with respect to the bias point V_{BIAS} $f_V = f_r$ and phase error within PDA window: high impedance.
3	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	F_{IN}	The input to the main counters, normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
5	V_{SS}	Negative supply (ground).
6	V_{DD}	Positive supply.
7, 8	$\overline{OSC\ IN}$/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external reference signal may, alternatively, be applied to $\overline{OSC\ IN}$. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047, with the division ratio being twice the programmed number.
9,10, 11, 12	D0-D3	Information on these inputs is transferred to the internal data latches during the appropriate data read time slot. D3 is MSB, D0 is LSB.
13	$\overline{ME}$	An open drain output for use in controlling the power supply to an external ROM or PROM. $\overline{ME}$ is low during the data read period and high impedance at other times.
14	PE	A positive or negative pulse or edge AC-coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner.
15, 16, 17	DS0-DS2	Internally generated three-state data select outputs, which may be used to address external memory.
18	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$, where P and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geqslant A$. Where every possible channel is required, the minimum total division ratio should be P^2-P.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

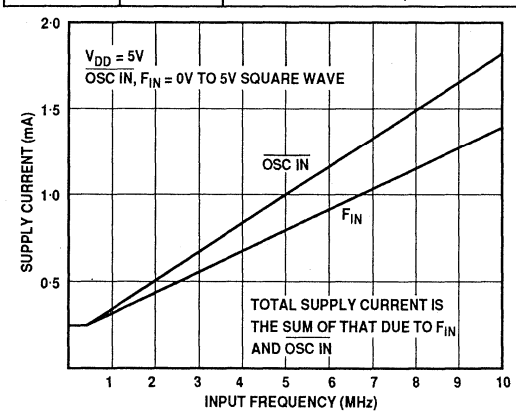


Fig. 3 Typical supply current v. input frequency

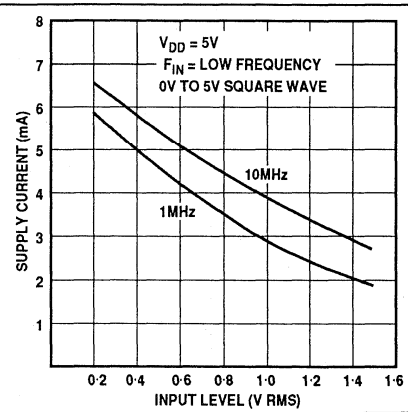


Fig. 4 Typical supply current v. input level, $\overline{OSC\ IN}$

PROGRAMMING

Program information can be obtained from an external ROM or PROM under the control of the NJ8820. Twenty-eight data bits are required per channel arranged as eight 4-bit words leaving four redundant bits, two of which are available on the data bus driving the data transfer time slot and may be used for external control purposes. A suitable PROM would be the 74S287, giving up to 32 channel capability as shown in Fig. 5. Note that the choice of PNP transistor and supply bypass capacitor on the ROM should be such that the ROM will power up in time: for example, at 10MHz oscillator frequency, the ROM must be powered up in less than 25μs.

Reading this data is normally done in single shot mode, with the data read cycle started by either a positive or negative pulse on the program enable (PE) pin. The data read cycle is generated from a program clock at 1/64 of the reference oscillator frequency. A memory enable signal ($\overline{ME}$) is supplied to allow power-down of the ROM when it is not in use. Data select outputs (DS0-DS2) remain in a high impedance state when the program cycle is completed to allow the address bus to be used for other functions if desired. The data map, data read cycle and timing diagram are shown in Figs. 6 to 8. Data is latched internally during the portions of the program cycle shown shaded in Fig. 7 and all data is transferred to the counters and latched during the data transfer time slot.

Alternatively, the PE pin may be grounded, causing the data read cycle to repeat cyclically to allow continuous up-dating of the program information. In this mode, external memory will be enabled continuously ($\overline{ME}$ low) and the data read cycle will repeat every sixteen cycles of the internal program clock, i.e. every $1024/f_{osc}$ seconds. This programming method is not recommended because the higher power consumption and the possibilities of noise into the loop from the digital data lines.

Power-on Programming

On power-up, the data read cycle is automatically initiated, making it unnecessary to provide a PE pulse. The circuit detects the power supply rising above a threshold point (nominally 1·5V) and, after an internally generated delay to allow the supply to rise fully, the circuit is programmed in the normal way. This delay is generated by counting reference oscillator pulses and is therefore dependent on the crystal used. The delay consists of 53248 reference oscillator cycles, giving a delay of about 5ms at 10MHz.

To ensure correct operation of this function, the power supply rise time should be less than 5ms (at 10MHz), rising smoothly through the threshold point.

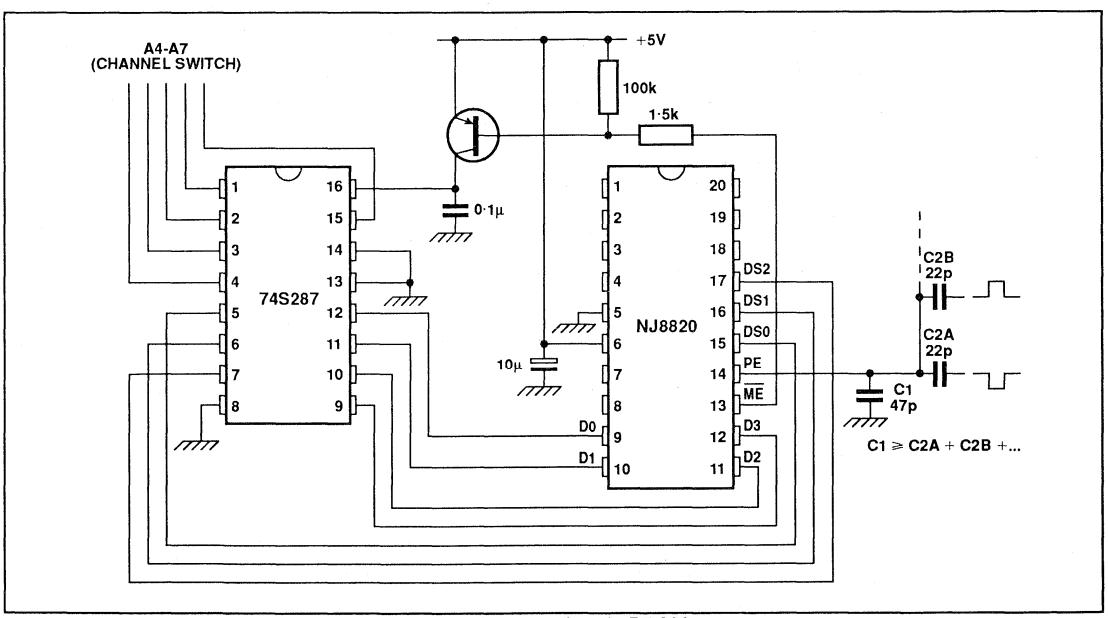


Fig. 5 Programming via PROM

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig. 6 Data map

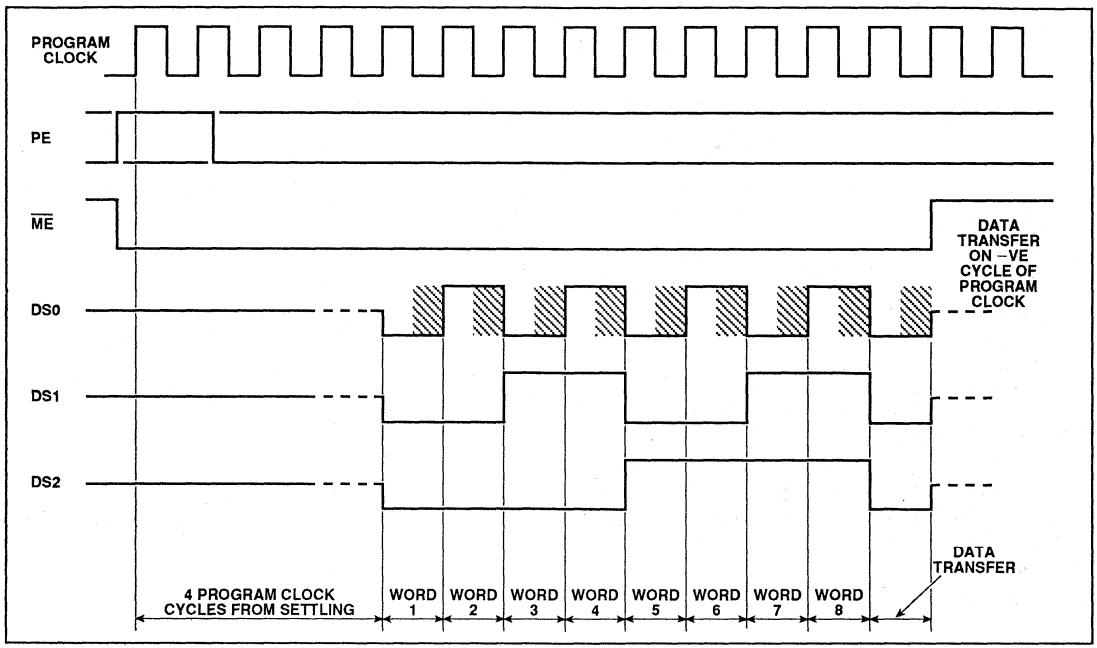


Fig.7 Data selection

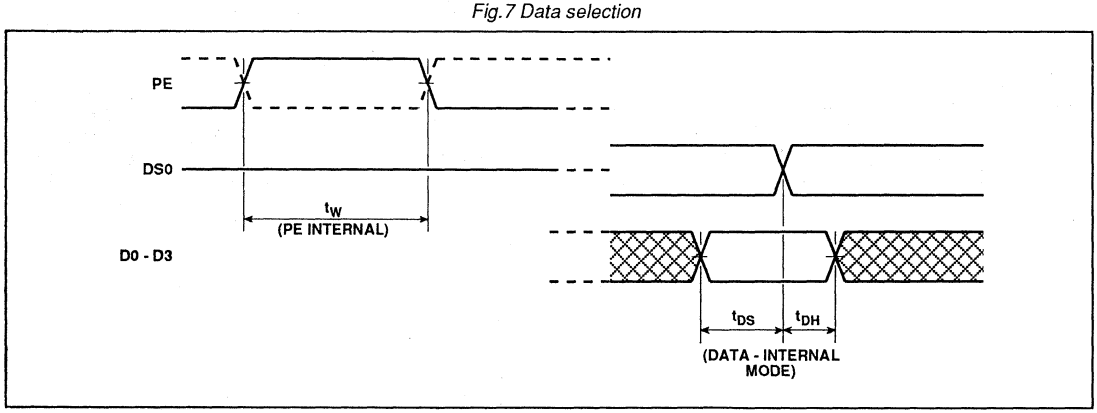


Fig.8 Timing diagram

PHASE COMPARATORS

The digital phase/frequency detector drives a three-state output, PDB, which provides a 'coarse' error signal to enable fast switching between channels. The PDB output is active until the phase error is within the sample and hold phase detector, PDA, window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on $\overline{LD}$. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset and the phase error is the phase comparator gain, which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between pin 8 (OSC OUT) and the other components. A value of 2·2kΩ is advised.

PROGRAMMING/POWER UP

Data and signal input pins should not have input applied to them prior to the application of V_{DD}, as otherwise latch-up may occur.

DS3278-1.3

NJ8821

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE) WITH RESETTABLE COUNTERS

The NJ8821 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor..

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8821 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of −30°C to +70°C. The NJ8821MA is available only in Ceramic DIL package with operating temperature range of −40°C to +85°C.

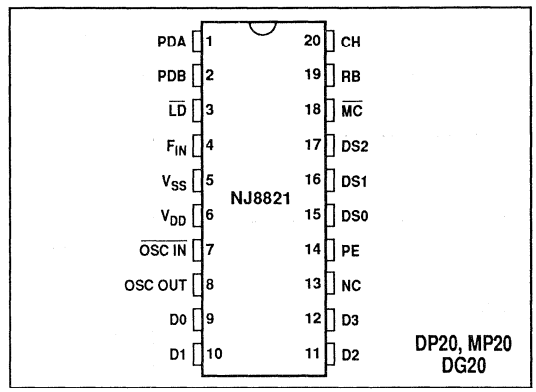


Fig.1 Pin connections - top view

FEATURES

- Low Power Consumption
- Microprocessor Compatible
- High Performance Sample and Hold Phase Detector
- >10MHz Input Frequency

ORDERING INFORMATION

NJ8821 BA DP Plastic DIL Package
NJ8821 BA MP Miniature Plastic DIL Package
NJ8821 MA DG Ceramic DIL Package

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}-V_{SS}$	−0·5V to 7V
Input voltage	
Open drain output, pin 3	7V
All other pins	V_{SS}−0·3V to V_{DD}+0·3V
Storage temperature	−65°C to +150°C (DG package, NJ8821MA)
Storage temperature	−55°C to +125°C (DP and MP packages, NJ8821)

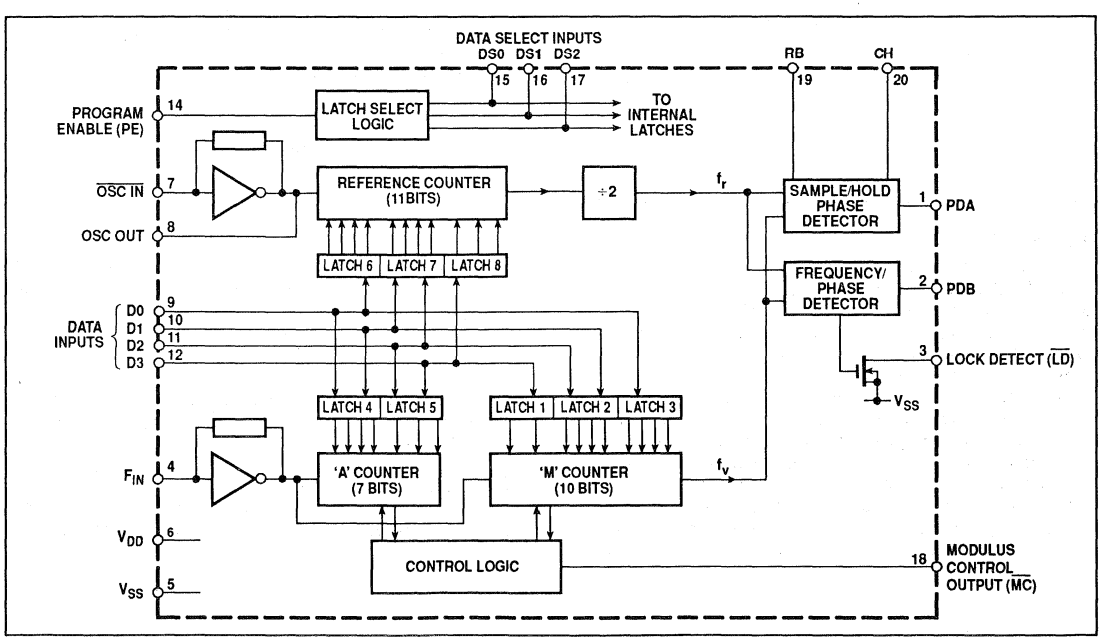


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS AT V_{DD} = 5V

Test conditions unless otherwise stated:

V_{DD}–V_{SS}=5V ±0·5V. Temperature range NJ8821 BA: –30°C to +70°C; NJ8821MA: –40°C to +85°C

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3·5	5·5	mA	f_{osc}, f_{FIN} = 10MHz } 0 to 5V square wave
		0·7	1·5	mA	f_{osc}, f_{FIN} = 1·0MHz }
OUTPUT LEVELS					
Modulus Control Output ($\overline{MC}$)					
High level	4·6			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 1mA
Lock Detect Output ($\overline{LD}$)					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7	V	
PDB Output					
High level	4·6			V	I_{SOURCE} = 5mA
Low level			0·4	V	I_{SINK} = 5mA
3-state leakage current			±0·1	µA	
INPUT LEVELS					
Data Inputs (D0-D3)					
High level	4·25			V	TTL compatible
Low level			0·4	V	See note 1
Program Enable Input (PE)					
High level	4·25			V	
Low level			0·75	V	
Data Select Inputs (DS0-DS2)					
High level	4·25			V	
Low level			0·75	V	

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
F_{IN} and $\overline{OSC\ IN}$ input level	200			mVRMS	10MHz AC-coupled sinewave
Max. operating frequency, f_{FIN} and f_{osc}	10·6			MHz	Input squarewave V_{DD} to V_{SS}, See note 4.
Propagation delay, clock to $\overline{MC}$		30	50	ns	See note 2.
Strobe pulse width, $t_{W(ST)}$	2			µs	} See Fig. 6
Data set-up time, t_{DS}	1			µs	
Data hold time, t_{DH}	1			µs	
Latch address set-up time, t_{SE}	1			µs	
Latch address hold time, t_{HE}	1			µs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See note 3.
Hold capacitor, CH			1	nF	
Output resistance, PDA			5	kΩ	
Digital phase detector gain		0·4		V/Rad	

NOTES

1. Data inputs have internal pull-up resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5µs, typically.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESCRIPTIONS

Pin no.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at $(V_{DD}-V_{SS})/2$ when the system is in lock. Voltage increases as f_v phase lead increases; voltage decreases as f_r phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB).
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v > f_r$ or f_v leading: positive pulses with respect to the bias point V_{BIAS} $f_v < f_r$ or f_r leading: negative pulses with respect to the bias point V_{BIAS} $f_v = f_r$ and phase error within PDA window: high impedance.
3	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	F_{IN}	The input to the main counters, normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
5	V_{SS}	Negative supply (ground).
6	V_{DD}	Positive supply.
7, 8	$\overline{OSC\ IN}$/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external reference signal may, alternatively, be applied to $\overline{OSC\ IN}$. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047, with the division ratio being twice the programmed number.
9,10, 11, 12	D0-D3	Data on these inputs is transferred to the internal data latches during the appropriate data read time slot. D3 is MSB, D0 is LSB.
13	NC	No connection
14	PE	This pin is used as a strobe for the data. A logic '1' on this pin transfers data from the D0-D3 pins to the internal latch addressed by the data select (DS0-DS2) pins . A logic '0' disables the data inputs.
15, 16, 17	DS0-DS2	Data select inputs for addressing the internal data latches
18	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$, where P and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geq A$. Where every possible channel is required, the minimum total division ratio should be P^2-P.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

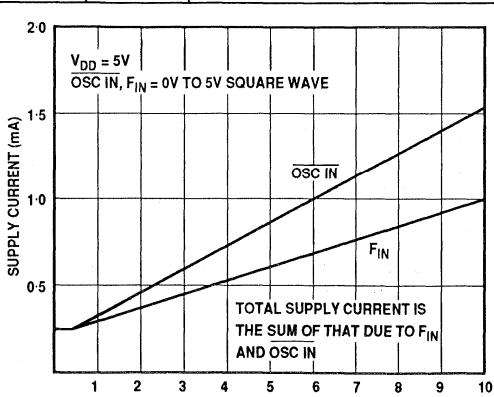


Fig. 3 Typical supply current v. input frequency

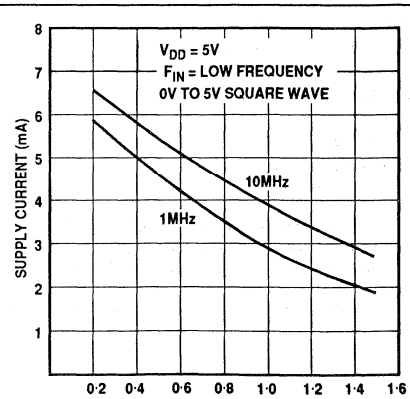


Fig. 4 Typical supply current v. input level, $\overline{OSC\ IN}$

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches as defined by the data map Fig.5. The PE pin is used as a strobe for the data: taking PE high causes data to be transferred from the data pins (D0-D3) into the addressed latch. Following the falling edge of PE, the data is retained in the addressed latch and the data inputs are disabled. Data transfer from all internal latches into the counters occurs simultaneously with the transfer of data into latch 1, which would therefore normally be the last latch addressed during each channel change. Timing information for this mode of operation is given in Fig. 6.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means that the synthesiser loop lock-up time is well defined and less than 10ms. If shorter lock-up times are are required when making only small changes in frequency, the GPS NJ8823 (with non-resettable counters) should be considered.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig. 5 Data map

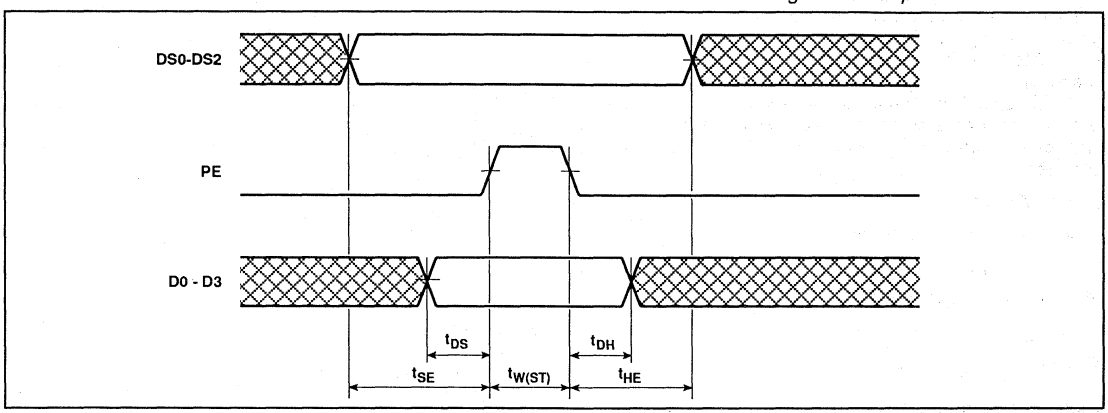


Fig. 6 Timing diagram

PHASE COMPARATORS

The digital phase/frequency detector drives a three-state output, PDB, which provides a 'coarse' error signal to enable fast switching between channels. The PDB output is active until the phase error is within the sample and hold phase detector, PDA, window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on $\overline{LD}$. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset and the phase error is the phase comparator gain, which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between pin 8 (OSC OUT) and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

Data and signal input pins should not have input applied to them prior to the application of V_{DD}, as otherwise latch-up may occur.

NJ88C22

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH RESETTABLE COUNTERS

The NJ88C22 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters, subsequent updating can be abbreviated to 17 bits, when only the 'A' and 'M' counters require changing.

The NJ88C22 is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8705 series to produce a universal binary coded synthesiser for up to 1100MHz operation.

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- >20MHz Input Frequency
- Fast Lock-up Time

ORDERING INFORMATION

NJ88C22 MA DG Ceramic DIL Package
NJ88C22 MA DP Plastic DIL Package
NJ88C22 MA MP Miniature Plastic DIL Package

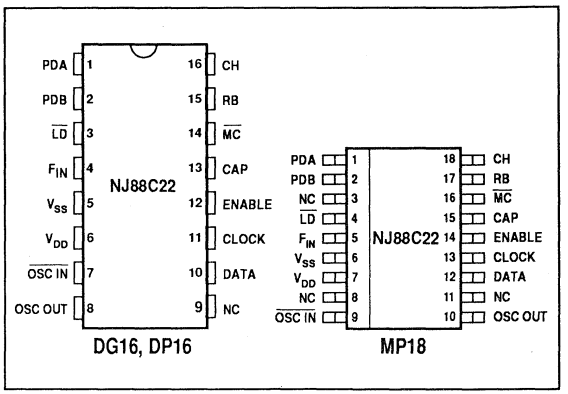


Fig.1 Pin connections - top view (not to scale)

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}-V_{SS}$:	−0·75V to 7V
Input voltage	
Open drain output, $\overline{LD}$ pin:	7V
All other pins:	$V_{SS}-0·3V$ to $V_{DD}+0·3V$
Storage temperature:	−55°C to +125°C (DP and MP packages)
	−65°C to +150°C (DG package)

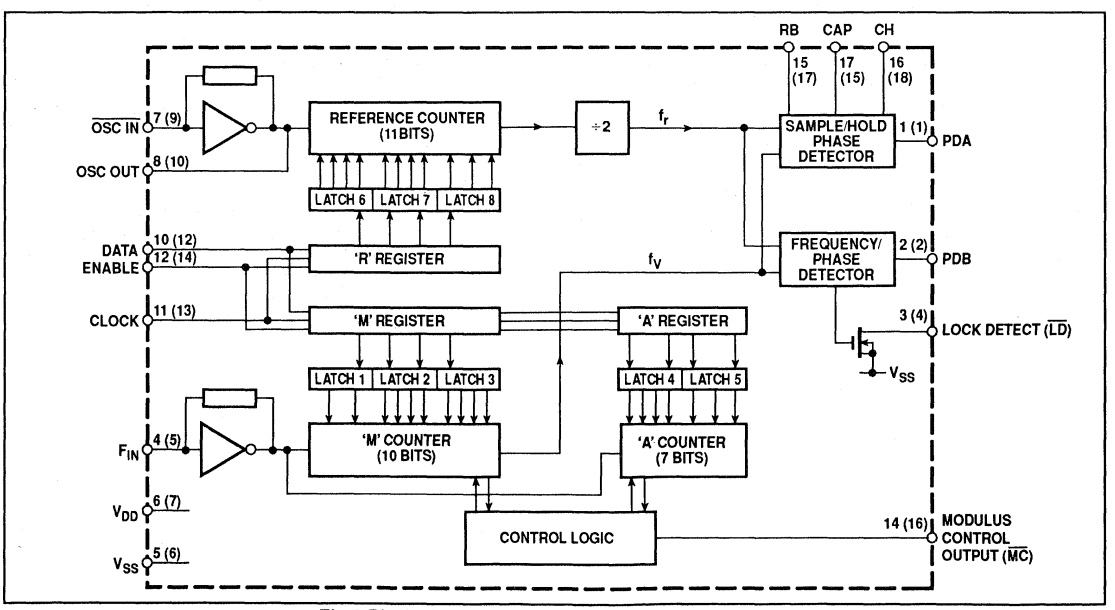


Fig.2 Block diagram (MP pinout shown in parentheses)

ELECTRICAL CHARACTERISTICS AT V_{DD} = 5V

Test conditions unless otherwise stated:

V_{DD}–V_{SS}=5V ±0·5V. Temperature range = –40°C to +85°C

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current			5·5	mA	f_{osc}, f_{FIN} = 10MHz } 0 to 5V square wave
			1.5	mA	f_{osc}, f_{FIN} = 1MHz }
Modulus Control Output ($\overline{MC}$)					
High level	4·6			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 1mA
Lock Detect Output ($\overline{LD}$)					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7·0	V	
PDB Output					
High level	4·6			V	I_{SOURCE} = 5mA
Low level			0·4	V	I_{SINK} = 5mA
3-state leakage current			±0·1	µA	

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
F_{IN} and $\overline{OSC\ IN}$ input level	200			mV RMS	10MHz AC-coupled sinewave
Max. operating frequency, f_{FIN} and f_{osc}	20			MHz	Input squarewave V_{DD} to V_{SS}, 25°C.
Propagation delay, clock to modulus control $\overline{MC}$		30	50	ns	See note 2
Programming Inputs					
Clock high time, t_{CH}	0·5			µs	} All timing periods are referenced to the negative transition of the clock waveform
Clock low time, t_{CL}	0·5			µs	
Enable set-up time, t_{ES}	0·2		t_{CH}	µs	
Enable hold time, t_{EH}	0·2			µs	
Data set-up time, t_{DS}	0·2			µs	
Data hold time, t_{DH}	0·2			µs	
Clock rise and fall times			0·2	µs	
High level threshold			V_{DD}–0·8	V	See note 1
Low level threshold	0·8			V	See note 1
Hysteresis	1·0			V	See note 1
Phase Detector					
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	See note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES

1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull-up resistors; they are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5µs.
4. The inputs to the device should be at logic '0' when power is applied if latch-up conditions are to be avoided. This includes the signal/osc. frequency inputs.

PIN DESCRIPTIONS

Pin no. DG,DP	Pin no. MP	Name	Description
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as f_v (the output from the 'M' counter) phase lead increases; voltage decreases as f_r (the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB). In a type 2 loop, this pin is at $(V_{DD}-V_{SS})/2$ when the system is in lock.
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v > f_r$ or f_v leading: positive pulses with respect to the bias point V_{BIAS} $f_v < f_r$ or f_r leading: negative pulses with respect to the bias point V_{BIAS} $f_v = f_r$ and phase error within PDA window: high impedance.
–	3	NC	Not connected.
3	4	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	5	F_{IN}	The input to the main counters. It is normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
5	6	V_{SS}	Negative supply (ground).
6	7	V_{DD}	Positive supply (normally 5V)
–	8	NC	Not connected.
7, 8	9,10	$\overline{OSC\ IN}$/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220Ω resistor between OSC OUT and the crystal will improve stability. An external reference signal may, alternatively, be applied to $\overline{OSC\ IN}$. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047 , with the total division ratio being twice the programmed number.
9	–	NC	Not connected.
10	12	DATA	Information on this input is transferred to the internal data latches during the appropriate data read time slot. DATA is high for a '1' and low for a '0'. There are three data words which control the NJ88C22; MSB is first in the order: 'A' (7 bits), 'M' (10 bits), 'R' (11 bits).
11	13	CLOCK	Data is clocked on the negative transition of the CLOCK waveform. If less than 28 negative clock transitions have been received when the ENABLE line goes low (i.e., only 'M' and 'A' will have been clocked in), then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded If 28 negative transitions have been counted, then the 'R' counter will be loaded with the new data.
12	14	ENABLE	When ENABLE is low, the DATA and CLOCK inputs are disabled internally. As soon as ENABLE is high, the DATA and CLOCK inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the ENABLE input and both inputs to the phase detector are synchronised to each other.
13	15	CAP	This pin allows an external capacitor to be connected in parallel with the internal ramp capacitor and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
14	16	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$, where P and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geq A$. Where every possible channel is required, the minimum total division ratio N should be: $N \geq P^2 - P$, where $N = MP+A$.
15	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
16	18	CH	An external hold capacitor should be connected between this pin and V_{SS}.

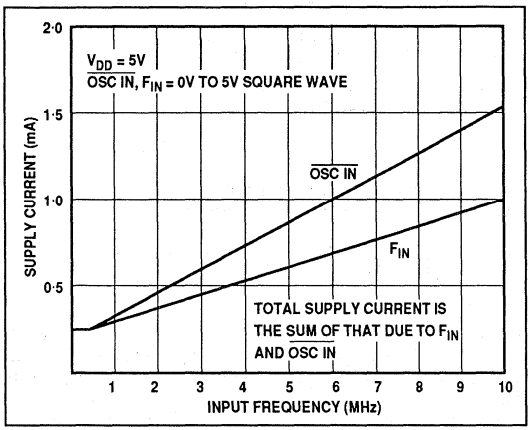


Fig. 3 Typical supply current v. input frequency

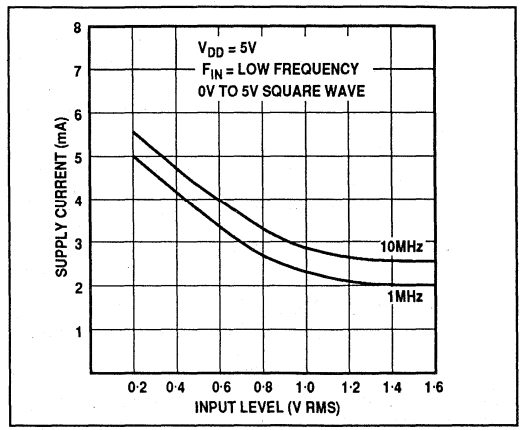


Fig. 4 Typical supply current v. input level, $\overline{OSC\ IN}$

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of th 'R' counter, which can be programmed in the range 3 to 2047, and a fixed divide by two stage.

$$R = \frac{fosc}{2 \times fcomp}$$

where *fosc* = oscillator frequency,
fcomp = comparison frequency,
R = 'R' counter ratio

For example, where the crystal frequency = 10MHz and a channel spacing comparison frequency of 12·5kHz is required,

$$R = \frac{10^7}{2 \times 12{\cdot}5 \times 10^3} = 400$$

Thus, the 'R' register would be programmed to 400 expressed in binary. The total division ratio would then be 2×400 = 800 since the total division ratio of the 'R' counter plus the ÷2 stage is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage controlled oscillator (VCO) will depend on the division ratios of the 'M' and 'A' counters, the ratio of the external two-modulus prescaler (*P/P+1*)and the comparison frequency .

The division ratio $N = MP+A$,
where *M* is the ratio of the 'M' counter in the range 8 to 1023 and *A* is the ratio of the 'A' counter in the range 0 to 127.

Note that $M \geqslant A$ and

$$N = \frac{f_{VCO}}{fcomp}$$

For example, if the desired VCO frequency = 275MHz, the comparison frequency is 12·5kHz and a two-modulus prescaler of ÷64/65 is being used, then

$$N = \frac{275 \times 10^6}{12{\cdot}5 \times 10^3} = 22 \times 10^3$$

Now, $N = MP+A$, which can be rearranged as $N/P = M+A/P$.
In our example we have $P = 64$, therefore

$$\frac{22 \times 10^3}{64} = M + \frac{A}{64}$$

such that $M = 343$ and $A/64 = 0{\cdot}75$.
Now, *M* is programmed to the integer part = 343 and *A* is programmed to the fractional part×64 i.e., $A = 0{\cdot}75 \times 64 = 48$.
NB The minimum ratio *N* that can be used is P^2-P (= 4032 in our example) for all contiguous channels to be available.

To check: $N = 343 \times 64 + 48 = 22000$, which is the required division ratio and is greater than 4032 ($= P^2-P$).

When re-programming, a reset to zero is followed by reloading with the new counter values, which means that the loop lock-up time will be well defined and less than 10ms. If shorter lock-up times are required, when making only small changes in frequency, the non-resettable NJ88C28 should be considered.

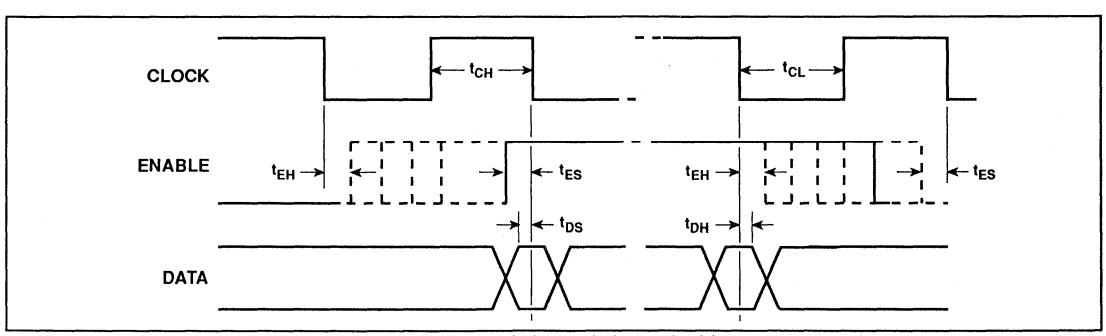


Fig. 5 Timing diagram showing timing periods required for correct operation

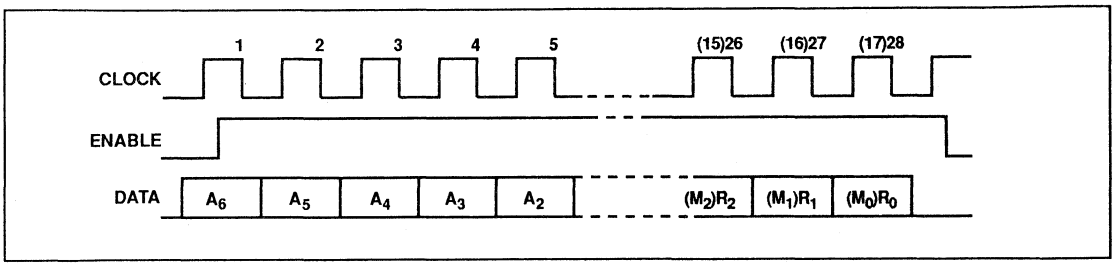


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain:

$$\frac{K_{PD}\,K_{VCO}}{N}$$

where K_{PD} is the phase detector constant (volts/rad), K_{VCO} is the VCO constant (rad/sec/volt) and N is the overall loop division ratio. When N is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase comparator in the NJ88C22 has a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output, PDB, provides a 'coarse' error signal to enable fast switching between channels.

The PDB output is active until the phase error is within the sample and hold phase detector window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on $\overline{LD}$. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock. An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset and the phase error is the phase comparator gain, K_{PDA}, which is programmable with an external resistor, RB, and a capacitor, CAP. An internal 50pF capacitor is used in the sample and hold comparator.

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between the OSC OUT pin and the other components. A value of between 150Ω and 270Ω is advised, depending on the crystal series resistance.

PROGRAMMING/POWER UP

Data and signal input pins should not have input applied to them prior to the application of V_{DD}, as otherwise latch-up may occur.

DS3279-1.3

NJ8823

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE) WITH NON-RESETTABLE COUNTERS

The NJ8823 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor..

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8823 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of −30°C to +70°C. The NJ8823MA is available only in Ceramic DIL package with operating temperature range of −40°C to +85°C.

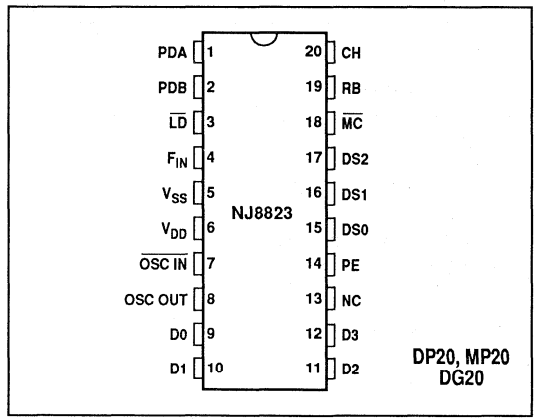


Fig.1 Pin connections - top view

FEATURES

- Low Power Consumption
- Microprocessor Compatible
- High Performance Sample and Hold Phase Detector
- >10MHz Input Frequency
- Fast Lock-up Time

ORDERING INFORMATION

NJ8823 BA DP Plastic DIL Package
NJ8823 BA MP Miniature Plastic DIL Package
NJ8823 MA DG Ceramic DIL Package

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}-V_{SS}$	−0·5V to 7V
Input voltage	
Open drain output, pin 3	7V
All other pins	V_{SS}−0·3V to V_{DD}+0·3V
Storage temperature	−65°C to +150°C (DG package, NJ8823MA)
Storage temperature	−55°C to +125°C (DP and MP packages, NJ8823)

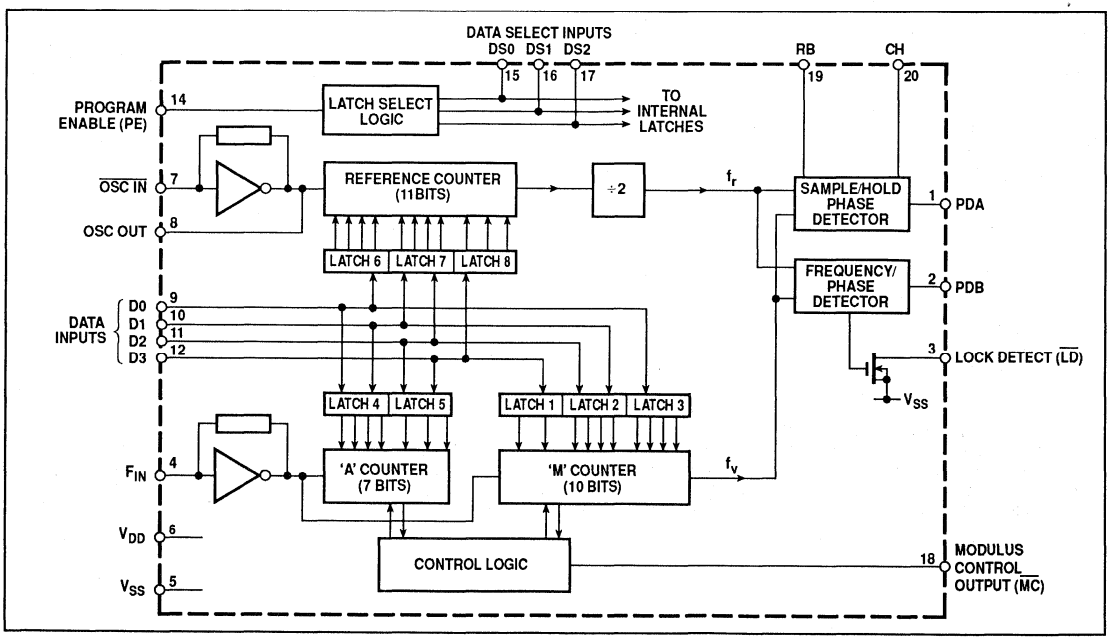


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS AT V_{DD} = 5V

Test conditions unless otherwise stated:

V_{DD}–V_{SS}=5V ±0·5V. Temperature range NJ8823 BA: –30°C to +70°C; NJ8823 MA: –40°C to +85°C

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3·5	5·5	mA	f_{OSC}, f_{FIN} = 10MHz } 0 to 5V square wave
		0·7	1·5	mA	f_{OSC}, f_{FIN} = 1·0MHz }
OUTPUT LEVELS					
Modulus Control Output ($\overline{MC}$)					
High level	4·6			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 1mA
Lock Detect Output ($\overline{LD}$)					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7	V	
PDB Output					
High level	4·6			V	I_{SOURCE} = 5mA
Low level			0·4	V	I_{SINK} = 5mA
3-state leakage current			±0·1	µA	
INPUT LEVELS					
Data Inputs (D0-D3)					
High level	4·25			V	TTL compatible
Low level			0·4	V	See note 1
Program Enable Input (PE)					
High level	4·25			V	
Low level			0·75	V	
Data Select Inputs (DS0-DS2)					
High level	4·25			V	
Low level			0·75	V	

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
F_{IN} and $\overline{OSC\ IN}$ input level	200			mVRMS	10MHz AC-coupled sinewave
Max. operating frequency, f_{FIN} and f_{osc}	10·6			MHz	Input squarewave V_{DD} to V_{SS}, See note 4.
Propagation delay, clock to $\overline{MC}$		30	50	ns	See note 2.
Strobe pulse width, $t_{W(ST)}$	2			µs	} See Fig. 6
Data set-up time, t_{DS}	1			µs	
Data hold time, t_{DH}	1			µs	
Latch address set-up time, t_{SE}	1			µs	
Latch address hold time, t_{HE}	1			µs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See note 3.
Hold capacitor, CH			1	nF	
Output resistance, PDA			5	kΩ	
Digital phase detector gain		0·4		V/Rad	

NOTES

1. Data inputs have internal pull-up resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5µs, typically.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESCRIPTIONS

Pin no.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at $(V_{DD}-V_{SS})/2$ when the system is in lock. Voltage increases as f_V phase lead increases; voltage decreases as f_r phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB).
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_V > f_r$ or f_V leading: positive pulses with respect to the bias point V_{BIAS} $f_V < f_r$ or f_r leading: negative pulses with respect to the bias point V_{BIAS} $f_V = f_r$ and phase error within PDA window: high impedance.
3	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	F_{IN}	The input to the main counters, normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
5	V_{SS}	Negative supply (ground).
6	V_{DD}	Positive supply.
7, 8	$\overline{OSC\ IN}$/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external reference signal may, alternatively, be applied to $\overline{OSC\ IN}$. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047, with the division ratio being twice the programmed number.
9,10, 11, 12	D0-D3	Data on these inputs is transferred to the internal data latches during the appropriate data read time slot. D3 is MSB, D0 is LSB.
13	NC	No connection
14	PE	This pin is used as a strobe for the data. A logic '1' on this pin transfers data from the D0-D3 pins to the internal latch addressed by the data select (DS0-DS2) pins . A logic '0' disables the data inputs.
15, 16, 17	DS0-DS2	Data select inputs for addressing the internal data latches
18	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$, where P and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geq A$. Where every possible channel is required, the minimum total division ratio should be P^2-P.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

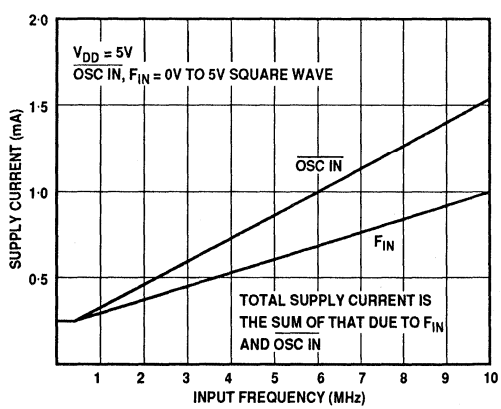


Fig. 3 Typical supply current v. input frequency

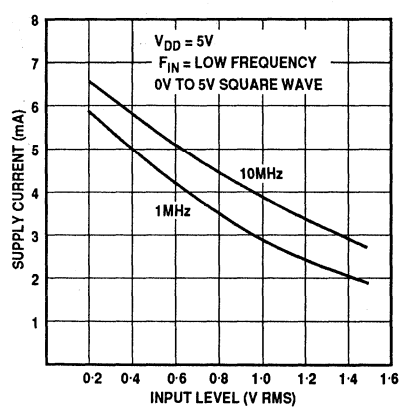


Fig. 4 Typical supply current v. input level, $\overline{OSC\ IN}$

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches as defined by the data map Fig.5. The PE pin is used as a strobe for the data: taking PE high causes data to be transferred from the data pins (D0-D3) into the addressed latch. Following the falling edge of PE, the data is retained in the addressed latch and the data inputs are disabled. Data transfer from all internal latches into the counters occurs simultaneously with the transfer of data into latch 1, which would therefore normally be the last latch addressed during each channel change. Timing information for this mode of operation is given in Fig. 6.

When re-programming, the counters are changed only when they reach a zero state. There is no reset to zero state, which means that the synthesiser loop lock-up time will be variable.

For the case when only small changes in frequency are required, the non-resettable synthesiser should achieve the shortest loop lock-up times.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig. 5 Data map

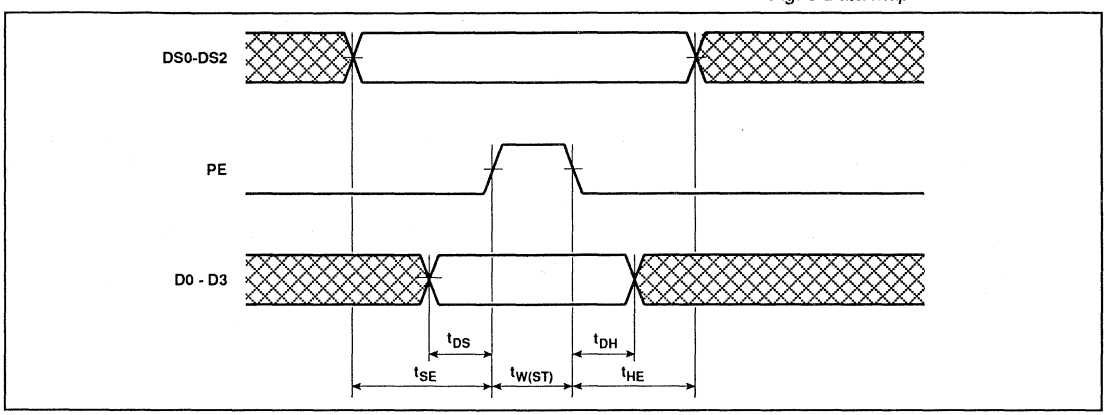


Fig. 6 Timing diagram

PHASE COMPARATORS

The digital phase/frequency detector drives a three-state output, PDB, which provides a 'coarse' error signal to enable fast switching between channels. The PDB output is active until the phase error is within the sample and hold phase detector, PDA, window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on $\overline{LD}$. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset and the phase error is the phase comparator gain, which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between pin 8 (OSC OUT) and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

Data and signal input pins should not have input applied to them prior to the application of V_{DD}, as otherwise latch-up may occur.

DS2438-2.3

NJ88C24

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH NON-RESETTABLE COUNTERS

The NJ88C24 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters, subsequent updating can be abbreviated to 17 bits, when only the 'A' and 'M' counters require changing.

The NJ88C24 is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8705 series to produce a universal binary coded synthesiser for up to 1100MHz operation.

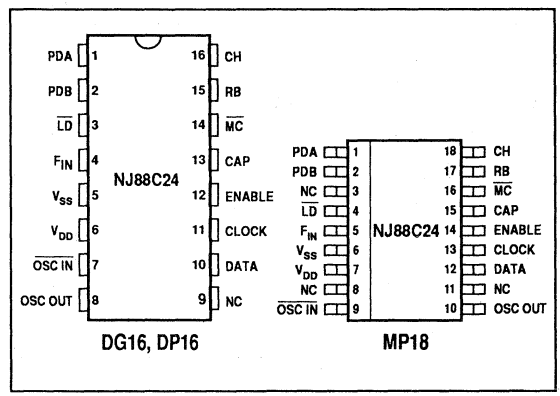


Fig.1 Pin connections - top view (not to scale)

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- >20MHz Input Frequency
- Fast Lock-up Time

ORDERING INFORMATION

NJ88C24 MA DG Ceramic DIL Package
NJ88C24 MA DP Plastic DIL Package
NJ88C24 MA MP Miniature Plastic DIL Package

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}-V_{SS}$:	−0·5V to 7V
Input voltage	
Open drain output, $\overline{LD}$ pin:	7V
All other pins:	$V_{SS}-0·3V$ to $V_{DD}+0·3V$
Storage temperature:	−55°C to +125°C (DP and MP packages)
	−65°C to +150°C (DG package)

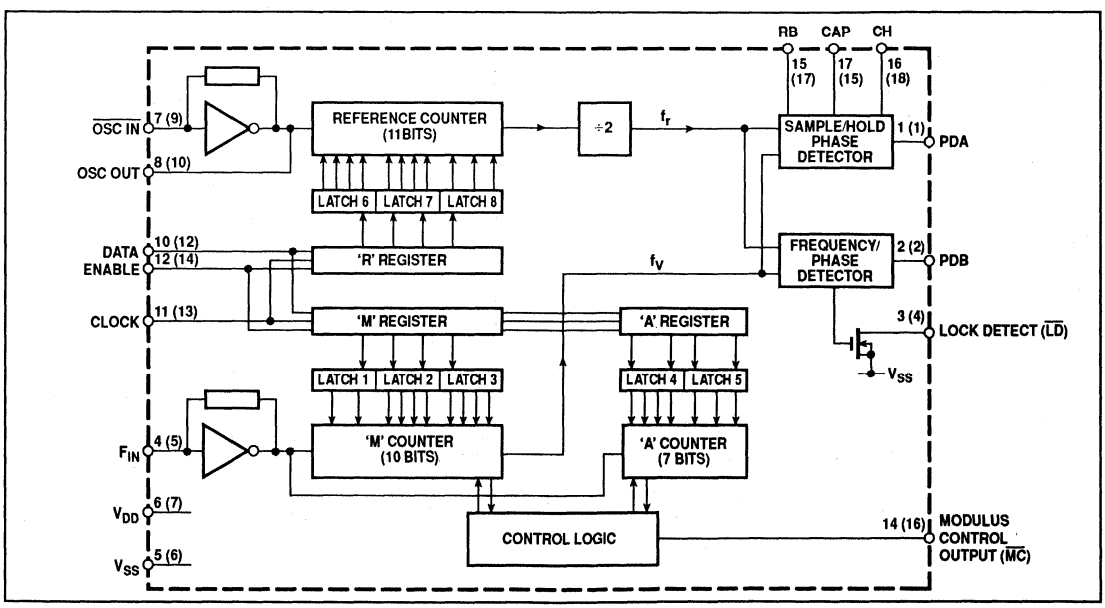


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS AT V_{DD} = 5V

Test conditions unless otherwise stated:

V_{DD}–V_{SS}=5V ±0·5V. Temperature range = –40°C to +85°C

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current			5·5	mA	f_{osc}, f_{FIN} = 10MHz } 0 to 5V square wave
			1.5	mA	f_{osc}, f_{FIN} = 1MHz }
Modulus Control Output ($\overline{MC}$)					
High level	4·6			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 1mA
Lock Detect Output ($\overline{LD}$)					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7·0	V	
PDB Output					
High level	4·6			V	I_{SOURCE} = 5mA
Low level			0·4	V	I_{SINK} = 5mA
3-state leakage current			±0·1	µA	

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
F_{IN} and $\overline{OSC\ IN}$ input level	200			mV RMS	10MHz AC-coupled sinewave
Max. operating frequency, f_{FIN} and f_{osc}	20			MHz	Input squarewave V_{DD} to V_{SS}, 25°C.
Propagation delay, clock to modulus control $\overline{MC}$		30	50	ns	See note 2
Programming Inputs					
Clock high time, t_{CH}	0·5			µs	} All timing periods are referenced to the negative transition of the clock waveform
Clock low time, t_{CL}	0·5			µs	
Enable set-up time, t_{ES}	0·2		t_{CH}	µs	
Enable hold time, t_{EH}	0·2			µs	
Data set-up time, t_{DS}	0·2			µs	
Data hold time, t_{DH}	0·2			µs	
Clock rise and fall times			0·2	µs	
High level threshold			V_{DD}–0·8	V	See note 1
Low level threshold	0·8			V	See note 1
Hysteresis	1·0			V	See note 1
Phase Detector					
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	See note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES

1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull-up resistors; they are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5µs.
4. The inputs to the device should be at logic '0' when power is applied if latch-up conditions are to be avoided. This includes the signal/osc. frequency inputs.

PIN DESCRIPTIONS

Pin no. DG,DP	Pin no. MP	Name	Description
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as f_V (the output from the 'M' counter) phase lead increases; voltage decreases as f_r (the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB). In a type 2 loop, this pin is at $(V_{DD}-V_{SS})/2$ when the system is in lock.
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_V > f_r$ or f_V leading: positive pulses with respect to the bias point V_{BIAS} $f_V < f_r$ or f_r leading: negative pulses with respect to the bias point V_{BIAS} $f_V = f_r$ and phase error within PDA window: high impedance.
–	3	NC	Not connected.
3	4	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	5	F_{IN}	The input to the main counters. It is normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
5	6	V_{SS}	Negative supply (ground).
6	7	V_{DD}	Positive supply (normally 5V)
–	8	NC	Not connected.
7, 8	9,10	$\overline{OSC\ IN}$/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220Ω resistor between OSC OUT and the crystal will improve stability. An external reference signal may, alternatively, be applied to $\overline{OSC\ IN}$. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047 , with the total division ratio being twice the programmed number.
9	–	NC	Not connected.
10	12	DATA	Information on this input is transferred to the internal data latches during the appropriate data read time slot. DATA is high for a '1' and low for a '0'. There are three data words which control the NJ88C24; MSB is first in the order: 'A' (7 bits), 'M' (10 bits), 'R' (11 bits).
11	13	CLOCK	Data is clocked on the negative transition of the CLOCK waveform. If less than 28 negative clock transitions have been received when the ENABLE line goes low (i.e., only 'M' and 'A' will have been clocked in), then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded If 28 negative transitions have been counted, then the 'R' counter will be loaded with the new data.
12	14	ENABLE	When ENABLE is low, the DATA and CLOCK inputs are disabled internally. As soon as ENABLE is high, the DATA and CLOCK inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the ENABLE input and both inputs to the phase detector are synchronised to each other.
13	15	CAP	This pin allows an external capacitor to be connected in parallel with the internal ramp capacitor and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
14	16	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$, where P and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geqslant A$. Where every possible channel is required, the minimum total division ratio N should be: $N \geqslant P^2-P$, where $N = MP+A$.
15	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
16	18	CH	An external hold capacitor should be connected between this pin and V_{SS}.

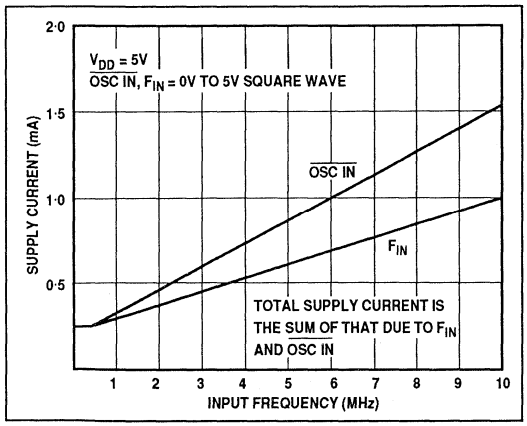


Fig. 3 Typical supply current v. input frequency

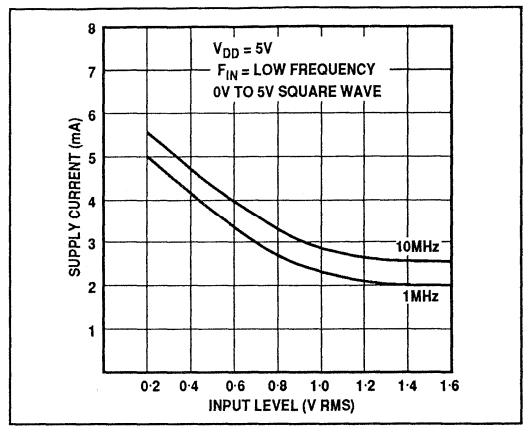


Fig. 4 Typical supply current v. input level, OSC IN

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of th 'R' counter, which can be programmed in the range 3 to 2047, and a fixed divide by two stage.

$$R = \frac{fosc}{2 \times fcomp}$$

where *fosc* = oscillator frequency,
fcomp = comparison frequency,
R = 'R' counter ratio

For example, where the crystal frequency = 10MHz and a channel spacing comparison frequency of 12·5kHz is required,

$$R = \frac{10^7}{2 \times 12{\cdot}5 \times 10^3} = 400$$

Thus, the 'R' register would be programmed to 400 expressed in binary. The total division ratio would then be 2×400 = 800 since the total division ratio of the 'R' counter plus the ÷2 stage is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage controlled oscillator (VCO) will depend on the division ratios of the 'M' and 'A' counters, the ratio of the external two-modulus prescaler (*P*/*P*+ *1*)and the comparison frequency .

The division ratio $N = MP+A$,

where *M* is the ratio of the 'M' counter in the range 8 to 1023 and *A* is the ratio of the 'A' counter in the range 0 to 127.

Note that $M \geqslant A$ and

$$N = \frac{f_{VCO}}{fcomp}$$

For example, if the desired VCO frequency = 275MHz, the comparison frequency is 12·5kHz and a two-modulus prescaler of ÷64/65 is being used, then

$$N = \frac{275 \times 10^6}{12{\cdot}5 \times 10^3} = 22 \times 10^3$$

Now, $N = MP+A$, which can be rearranged as $N/P = M+A/P$. In our example we have $P = 64$, therefore

$$\frac{22 \times 10^3}{64} = M + \frac{A}{64}$$

such that $M = 343$ and $A/64 = 0{\cdot}75$.

Now, *M* is programmed to the integer part = 343 and *A* is programmed to the fractional part×64 i.e., $A = 0{\cdot}75 \times 64 = 48$.

NB The minimum ratio *N* that can be used is P^2-P (=4032 in our example) for all contiguous channels to be available.

To check: $N = 343 \times 64 + 48 = 22000$, which is the required division ratio and is greater than 4032 ($= P^2-P$).

When re-programming, the counters are changed only at the zero state. There is no reset to zero , which means that the synthesiser loop lock-up time will be variable. When only small changes in frequency are required, the non-resettable synthesiser should achieve the shortest loop lock-up times.

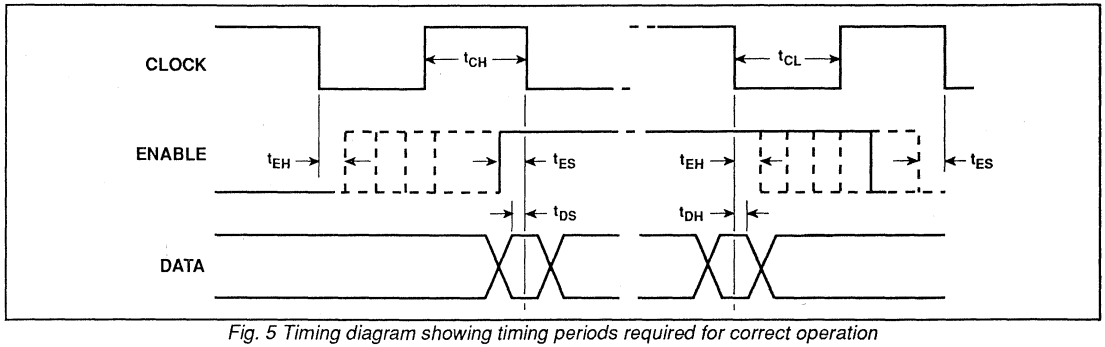


Fig. 5 Timing diagram showing timing periods required for correct operation

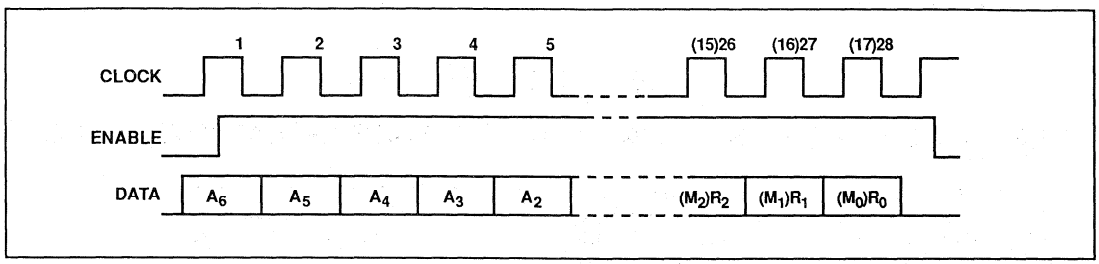


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain:

$$\frac{K_{PD}\,K_{VCO}}{N}$$

where K_{PD} is the phase detector constant (volts/rad), K_{VCO} is the VCO constant (rad/sec/volt) and N is the overall loop division ratio. When N is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase comparator in the NJ88C24 has a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output,PDB, provides a 'coarse' error signal to enable fast switching between channels.

The PDB output is active until the phase error is within the sample and hold phase detector window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on $\overline{LD}$. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock. An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset and the phase error is the phase comparator gain, K_{PDA}, which is programmable with an external resistor, RB, and a capacitor, CAP. An internal 50pF capacitor is used in the sample and hold comparator.

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between the OSC OUT pin and the other components. A value of between 150Ω and 270Ω is advised, depending on the crystal series resistance.

PROGRAMMING/POWER UP

Data and signal input pins should not have input applied to them prior to the application of V_{DD}, as otherwise latch-up may occur.

NJ88C25

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE)

The NJ88C25 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter, latched and buffered Band 0 and Band 1 outputs and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 30 bits of data are initially required to program all counters, subsequent updating can be abbreviated to 19 bits, when only the 'A', 'M' and 'B' counters require changing.

The NJ88C25 is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

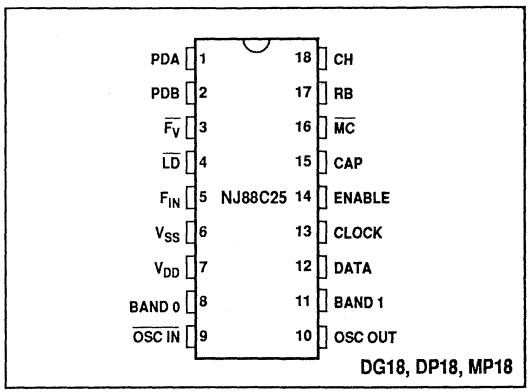


Fig.1 Pin connections - top view

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature

ORDERING INFORMATION

NJ88C25 KA DG Ceramic DIL Package
NJ88C25 KA DP Plastic DIL Package
NJ88C25 KA MP Miniature Plastic DIL Package

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}-V_{SS}$: −0·5V to 7V
Input voltage
Open drain output, pins 3 and 4: 7V
All other pins: $V_{SS}-0{\cdot}3V$ to $V_{DD}+0{\cdot}3V$
Storage temperature: −65°C to +150°C (DG package)
−55°C to +125°C (DP and MP packages)

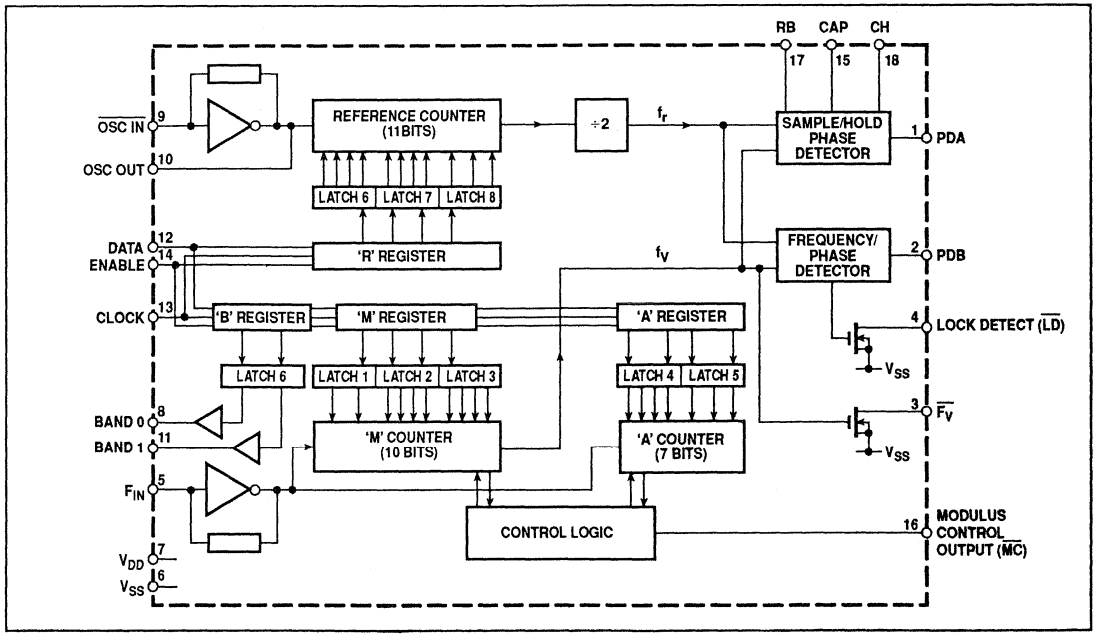


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS AT V_{DD} = 5V

Test conditions unless otherwise stated:

V_{DD}–V_{SS}=2·7V to 5·5V. Temperature range = –30°C to +70°C

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5·5		mA	f_{osc}, f_{FIN} = 20MHz } 0 to 5V
		0·7		mA	f_{osc}, f_{FIN} = 1MHz } square
		3·7		mA	f_{osc}, f_{FIN} = 10MHz } wave
OUTPUTS					
Modulus Control ($\overline{MC}$), BAND 1 and BAND 2					
High level	V_{DD}–0·4			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 1mA
Lock Detect ($\overline{LD}$) and $\overline{F_V}$					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7·0	V	
PDB					
High level	4·6			V	I_{SOURCE} = 4mA
Low level			0·4	V	I_{SINK} = 4mA
3-state leakage current			±0·1	μA	

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
F_{IN} and $\overline{OSC\ IN}$ input level	200			mV RMS	10MHz AC-coupled sinewave
Max. operating frequency, f_{FIN} and f_{osc}	20			MHz	Input squarewave V_{DD} to V_{SS},
Propagation delay, clock to modulus control $\overline{MC}$		30	50	ns	See note 2
Programming Inputs					
Clock high time, t_{CH}	0·5			μs	} All timing periods
Clock low time, t_{CL}	0·5			μs	} are referenced to
Enable set-up time, t_{ES} (see note 5)	0·2		t_{CH}	μs	} the negative
Enable hold time, t_{EH}	0·2			μs	} transition of the
Data set-up time, t_{DS}	0·2			μs	} clock waveform.
Data hold time, t_{DH}	0·2			μs	} See note 5
Clock rise and fall times	0·2			μs	}
Positive threshold	3			V	} TTL compatible, see note 1
Negative threshold			2	V	}
Phase Detector					
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	See note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES

1. Data inputs have internal pull-up resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5μs.
4. The inputs to the device should be at logic '0' when power is applied if latch-up conditions are to be avoided. This includes the $\overline{OSC\ IN}$ and F_{IN} inputs.
5. Clock to enable set-up time (t_{ES}) is variable, dependent on f_{osc}. It needs to be specified in terms of f_{osc}, clock high time (t_{CH}) and clock low time (t_{CL}) and must meet the following conditions: $4\times1/f_{osc} \leq t_{ES} < (t_{CH}+t_{CL})$.

PIN DESCRIPTIONS

Pin no.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as f_v (the output from the 'M' counter) phase lead increases; voltage decreases as f_r (the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB). In a type 2 loop, this pin is at $(V_{DD}-V_{SS})/2$ when the system is in lock.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v > f_r$ or f_v leading: positive pulses with respect to the bias point V_{BIAS} $f_v < f_r$ or f_r leading: negative pulses with respect to the bias point V_{BIAS} $f_v = f_r$ and phase error within PDA window: high impedance.
3	$\overline{F_V}$	This pin is an open drain output from the 'M' counter.
4	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
5	F_{IN}	The input to the main counters. It is normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
6	V_{SS}	Negative supply (ground).
7	V_{DD}	Positive supply (normally 5V)
9,10	$\overline{OSC\ IN}$/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220Ω resistor between OSC $\overline{OUT}$ and the crystal will improve stability. An external reference signal may, alternatively, be applied to $\overline{OSC\ IN}$. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047 , with the total division ratio being twice the programmed number.
8, 11	BAND 0/1	Two latch outputs, providing an output of the data from the 'B' register.
12	DATA	Information on this input is transferred to the internal data latches during the appropriate data read time slot. DATA is high for a '1' and low for a '0'. There are four data words which control the NJ88C25; MSB is first in the order: 'A' (7 bits), 'M' (10 bits),]B' (2 bits) and 'R' (11 bits).
13	CLOCK	Data is clocked on the negative transition of the CLOCK waveform. If less than 30 negative clock transitions have been received when the ENABLE line goes low (i.e., only 'B','M' and 'A' will have been clocked in), then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'B', 'M' and 'A' have been loaded. If 30 negative transitions have been counted, then the 'R' counter will be loaded with the new data.
14	ENABLE	When ENABLE is low, the DATA and CLOCK inputs are disabled internally. As soon as ENABLE is high, the DATA and CLOCK inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the ENABLE input and both inputs to the phase detector are synchronised to each other.
15	CAP	This pin allows an external capacitor to be connected in parallel with the internal ramp capacitor and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
16	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$, where P and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 8-1023 and, for correct operation, $M \geq A$. Where every possible channel is required, the minimum total division ratio N should be: $N \geq P^2-P$.
17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
18	CH	An external hold capacitor should be connected between this pin and V_{SS}.

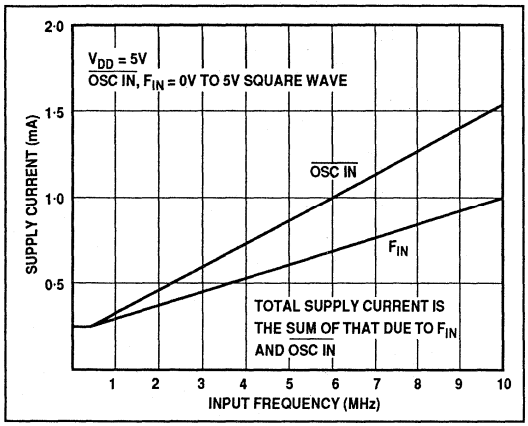


Fig. 3 Typical supply current v. input frequency

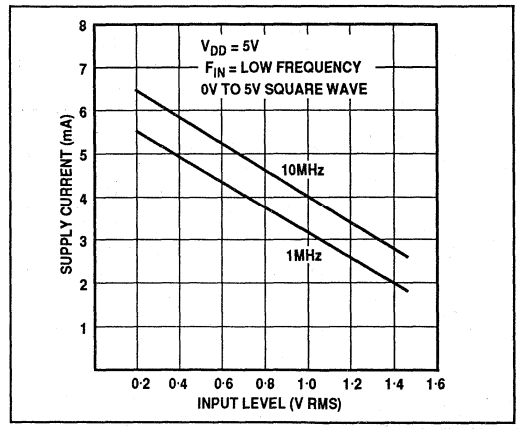


Fig. 4 Typical supply current v. input level, OSC IN

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of th 'R' counter, which can be programmed in the range 3 to 2047, and a fixed divide by two stage.

$$R = \frac{fosc}{2 \times fcomp}$$

where *fosc* = oscillator frequency,
fcomp = comparison frequency,
R = 'R' counter ratio

For example, where the crystal frequency = 10MHz and a channel spacing comparison frequency of 12·5kHz is required,

$$R = \frac{10^7}{2 \times 12{\cdot}5 \times 10^3} = 400$$

Thus, the 'R' register would be programmed to 400 expressed in binary. The total division ratio would then be 2×400 = 800 since the total division ratio of the 'R' counter plus the ÷2 stage is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage controlled oscillator (VCO) will depend on the division ratios of the 'M' and 'A' counters, the ratio of the external two-modulus prescaler (*P/P+1*)and the comparison frequency .

The division ratio $N = MP+A$,
where *M* is the ratio of the 'M' counter in the range 8 to 1023 and *A* is the ratio of the 'A' counter in the range 0 to 127. Note that $M \geqslant A$ and

$$N = \frac{f_{VCO}}{fcomp}$$

For example, if the desired VCO frequency = 275MHz, the comparison frequency is 12·5kHz and a two-modulus prescaler of ÷64/65 is being used, then

$$N = \frac{275 \times 10^6}{12{\cdot}5 \times 10^3} = 22 \times 10^3$$

Now, $N = MP+A$, which can be rearranged as $N/P = M+A/P$. In our example we have $P = 64$, therefore

$$\frac{22 \times 10^3}{64} = M + \frac{A}{64}$$

such that $M = 343$ and $A/64 = 0{\cdot}75$.
Now, *M* is programmed to the integer part = 343 and *A* is programmed to the fractional part×64 i.e., $A = 0{\cdot}75 \times 64 = 48$.
NB The minimum ratio *N* that can be used is P^2-P (=4032 in our example) for all contiguous channels to be available.

To check: $N = 343 \times 64 + 48 = 22000$, which is the required division ratio and is greater than 4032 ($= P^2-P$).

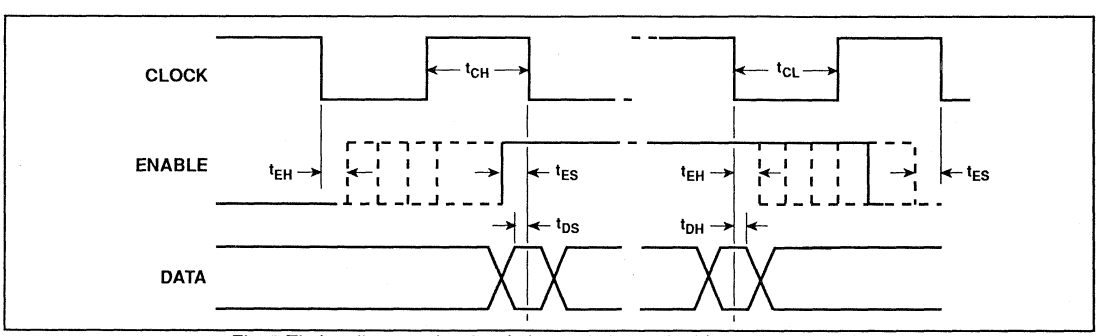


Fig. 5 Timing diagram showing timing periods required for correct operation

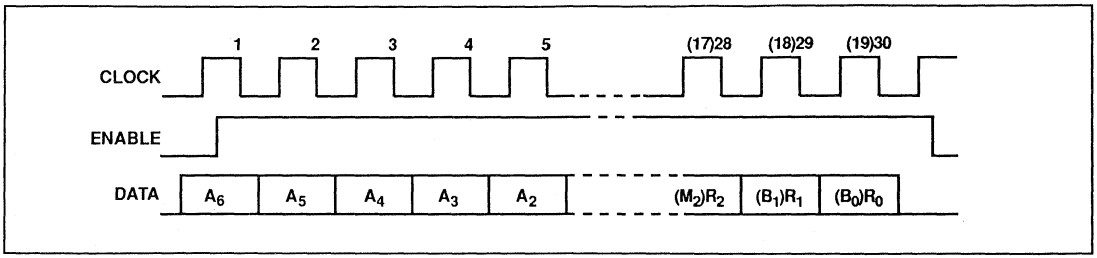


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain:

$$\frac{K_{PD}\,K_{VCO}}{N}$$

where K_{PD} is the phase detector constant (volts/rad), K_{VCO} is the VCO constant (rad/sec/volt) and N is the overall loop division ratio. When N is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase comparator in the NJ88C25 has a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output, PDB, provides a 'coarse' error signal to enable fast switching between channels.

The PDB output is active until the phase error is within the sample and hold phase detector window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on $\overline{LD}$. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock. An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset and the phase error is the phase comparator gain, K_{PDA}, which is programmable with an external resistor, RB, and a capacitor, CAP. An internal 50pF capacitor is used in the sample and hold comparator.

NJ88C28

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH NON-RESETTABLE COUNTERS

(Supersedes September 1991 Edition)

The NJ88C28 is a synthesiser circuit fabricated on the GPS CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters, subsequent updating can be abbreviated to 17 bits, when only the 'A' and 'M' counters require changing.

The NJ88C28 is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8705 series to produce a universal binary coded synthesiser for up to 1100MHz operation. Operation from a 3V supply is also supported.

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- 3V Operation
- Fast Lock Up Time
- SSOP Package Option

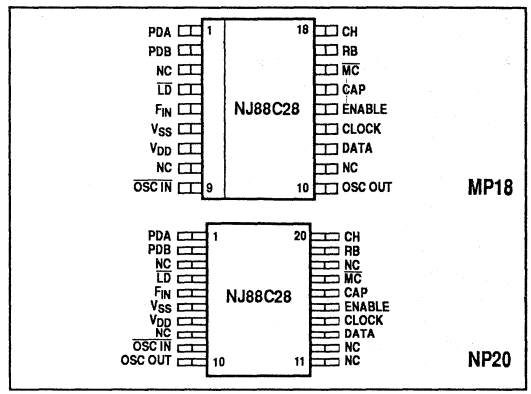


Fig.1 Pin connections - top view (not to scale)

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_{DD}-V_{SS}$	−0·75V to 7V
Input voltage	
Open drain output, pin 4	7V
All other pins	$V_{SS}-0·3V$ to $V_{DD}+0·3V$
Storage temperature	−55°C to +125°C

ORDERING INFORMATION

NJ88C28 IG MPES Miniature Plastic DIL Package
NJ88C28 IG NPAS Shrunk Miniature Plastic DIL Package

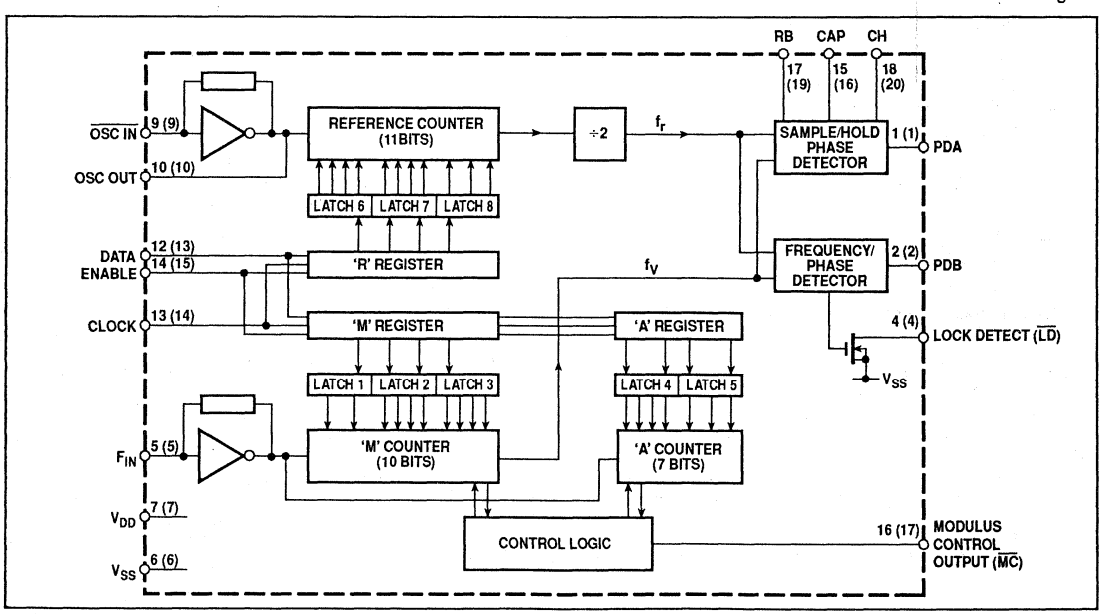


Fig.2 block diagram (NP pinout shown in parentheses)

ELECTRICAL CHARACTERISTICS AT V_{DD} = 5V

These characteristics are guaranteed over the following conditions, unless otherwise stated:

V_{DD}–V_{SS}=5V ±0·5V. Temperature range = –40°C to +85°C

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current			5·5	mA	f_{osc}, f_{FIN} = 10MHz } 0 to 5V square wave
		0.8		mA	f_{osc}, f_{FIN} = 4·096MHz }
Modulus Control Output ($\overline{MC}$)					
High level	4·6			V	I_{SOURCE} = 1mA
Low level			0·4	V	I_{SINK} = 1mA
Lock Detect Output ($\overline{LD}$)					
Low level			0·4	V	I_{SINK} = 4mA
Open drain pull-up voltage			7·0	V	
PDB Output					
High level	4·6			V	I_{SOURCE} = 5mA
Low level			0·4	V	I_{SINK} = 5mA
3-state leakage current			±100	nA	

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
F_{IN} and $\overline{OSC\ IN}$ input level	200			mV RMS	10MHz AC-coupled sinewave
Max. operating frequency, f_{FIN} and f_{osc}	20			MHz	Input squarewave V_{DD} to V_{SS}, 25°C. See note 5.
Propagation delay, clock to modulus control $\overline{MC}$		30	50	ns	See note 2
Programming Inputs					
Clock high time, t_{CH}	0·5			µs	All timing periods are referenced to the negative transition of the clock waveform
Clock low time, t_{CL}	0·5			µs	
Enable set-up time, t_{ES}	0·2		t_{CH}	µs	
Enable hold time, t_{EH}	0·2			µs	
Data set-up time, t_{DS}	0·2			µs	
Data hold time, t_{DH}	0·2			µs	
Clock rise and fall times			0·2	µs	
High level threshold			V_{DD}–0·8	V	See note 1
Low level threshold	0·8			V	See note 1
Hysteresis	1·0			V	See note 1
Phase Detector					See note 3
Positive going threshold, V_T+		1·0		V	
Negative going threshold, V_T–		1·4		V	
Digital phase detector propagation delay		500		ns	
RB current, I_{RB}	1		600	µA	Set by external conditions.
CAP/RB current gain, α	6·9	8·1	9·2		Over RB current range (±3σ).
Programming capacitor, CAP		53		pF	C_{int} plus packaging strays.
Output resistance, PDA, PDB		100		Ω	

NOTES

1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull-up resistors; they are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5µs, typically; 1µs for the sample and hold amplifier.
4. The inputs to the device should be at logic '0' when power is applied if latch-up conditions are to be avoided. This includes the signal/osc. frequency inputs.
5. The CAP reset device limits the minimum f_{in} period due to its time constant formed by the CAP pin's capacitance value. A typical $R_{DS(ON)}$ is about 1kΩ. Refer to AN112 for further details.

ELECTRICAL CHARACTERISTICS AT V_{DD}= 3V

These characteristics are guaranteed over the following conditions, unless otherwise stated:

V_{DD}–V_{SS}=3V, temperature range = –40°C to +85°C

DC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current				mA	f_{osc}, f_{FIN} = 10MHz } 0 to 3V square wave
		0·81		mA	f_{osc}, f_{FIN} = 4·096MHz }
Modulus Control Output ($\overline{MC}$)					
High level				V	I_{SOURCE} = 1mA
Low level				V	I_{SINK} = 1mA
Lock Detect Output ($\overline{LD}$)					
Low level				V	I_{SINK} = 4mA
Open drain pull-up voltage				V	
PDB Output					
High level				V	I_{SOURCE} = 5mA
Low level				V	I_{SINK} = 5mA
3-state leakage current				nA	

AC Characteristics

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
$\overline{OSC\ IN}$ input level	200			mV RMS	12·8MHz AC-coupled sinewave
F_{IN} input level	200			mV RMS	10MHz AC-coupled sinewave
Max. operating frequency, f_{FIN} and f_{osc}	20			MHz	Input squarewave V_{DD} to V_{SS}, 25°C. See note 5.
Propagation delay, clock to modulus control $\overline{MC}$		30	50	ns	See note 2
Programming Inputs					
Clock high time, t_{CH}	0·5			µs	All timing periods are referenced to the negative transition of the clock waveform
Clock low time, t_{CL}	0·5			µs	
Enable set-up time, t_{ES}	0·2		t_{CH}	µs	
Enable hold time, t_{EH}	0·2			µs	
Data set-up time, t_{DS}	0·2			µs	
Data hold time, t_{DH}	0·2			µs	
Clock rise and fall times			0·2	µs	
High level threshold			V_{DD}–0·8	V	See note 1
Low level threshold	0·8			V	See note 1
Hysteresis	1·0			V	See note 1
Phase Detector					See note 3
Positive going threshold, V_T+		0·8		V	
Negative going threshold, V_T–		1·1		V	
Digital phase detector propagation delay		500		ns	
RB current, I_{RB}	1		200	µA	Set by external conditions.
CAP/RB current gain, α	6·3	7·0	7·8		Over RB current range (±3σ).
Programming capacitor, CAP				pF	C_{int} plus packaging strays.
Output resistance, PDA, PDB		100		Ω	

NOTES

1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull-up resistors; they are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of the sample switch driving this pin will add a finite time constant to the loop. An external 1nF hold capacitor will give a maximum time constant of 5µs, typically; 1µs for the sample and hold amplifier.
4. The inputs to the device should be at logic '0' when power is applied if latch-up conditions are to be avoided. This includes the signal/osc. frequency inputs.
5. The CAP reset device limits the minimum f_{in} period due to its time constant formed by the CAP pin's capacitance value. A typical $R_{DS(ON)}$ is about 1kΩ. Refer to AN112 for further details.

PIN DESCRIPTIONS

Pin no. NP	Pin no. MP	Name	Description
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as f_v (the output from the 'M' counter) phase lead increases; voltage decreases as f_r (the output from the 'R' counter) phase lead increases. Output is linear over only a narrow phase window, determined by gain (programmed by RB). This pin is at $(V_{DD}-V_{SS})/2$ when the system is in lock, for an external loop filter amplifier biased to $(V_{DD}-V_{SS})/2$. Ideally, V_{BIAS} should be chosen such that the PDA window is centred between the thresholds, typically at $0{\cdot}55(V_{DD}-V_{SS})$
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. $f_v > f_r$ or f_v leading: positive pulses with respect to the bias point V_{BIAS} $f_v < f_r$ or f_r leading: negative pulses with respect to the bias point V_{BIAS} $f_v = f_r$ and phase error within PDA window: high impedance. (Minimum, $M = 3$ for correct function of PDB).
3	3	NC	Not connected..
4	4	$\overline{LD}$	An open-drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
5	5	F_{IN}	The input to the main counters. It is normally driven from a prescaler, which may be AC-coupled or, when a full logic swing is available, may be DC-coupled.
6	6	V_{SS}	Negative supply (ground).
7	7	V_{DD}	Positive supply.
8	8	NC	Not connected.
9,10	9,10	$\overline{OSC\ IN}$/ OSC OUT	These pins form an on-chip reference oscillator when a series resonant crystal is connected across them. Capacitors of appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 2·2kΩ resistor between pin 10 and the crystal will improve stability. An external reference signal may, alternatively, be applied to $\overline{OSC\ IN}$. This may be a low-level signal, AC-coupled, or if a full logic swing is available it may be DC-coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the total division ratio being twice the programmed value i.e., 6 to 4094 in steps of 2.
11	11	NC	Not connected.
12	–	NC	Not connected.
13	12	DATA	Information on this input is transferred to the internal data latches during the appropriate data read time slot. DATA is high for a '1' and low for a '0'. There are three data words which control the NJ88C28; MSB is first in the order: 'A' (7 bits), 'M' (10 bits), 'R' (11 bits).
14	13	CLOCK	Data is clocked on the negative transition of the CLOCK waveform. If less than 28 negative clock transitions have been received when the ENABLE line goes low (i.e., only 'M' and 'A' will have been clocked in), then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. If 28 negative transitions have been counted, then the 'R' counter will be loaded with the new data.
15	14	ENABLE	When ENABLE is low, the DATA and CLOCK inputs are disabled internally. As soon as ENABLE is high, the DATA and CLOCK inputs are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the ENABLE input and both inputs to the phase detector are synchronised to each other.
16	15	CAP	This pin allows an external capacitor to be connected in parallel with the internal ramp capacitor and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
17	16	$\overline{MC}$	Modulus control output for controlling an external dual-modulus prescaler. $\overline{MC}$ will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. $\overline{MC}$ then goes high and remains high until the 'M' counter completes its cycle, at which point both 'A' and 'M' counters are reset. This gives a total division ratio of $MP+A$, where P and $P+1$ represent the dual-modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The programming range of the 'M' counter is 3-1023 but $M \geq 8$ for correct PDA operation and, for correct operation with a prescaler, $M \geq A$. Where every possible channel is required, the minimum total division ratio N should be: $N \geq P^2-P$, where $N = MP+A$.
18	–	NC	Not connected

PIN DESCRIPTIONS (continued)

Pin no. NP	Pin no. MP	Name	Description
19	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}. I_{RB} <600μA at V_{DD} = 5V.
20	18	CH	An external hold capacitor should be connected between this pin and V_{SS}.

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of th 'R' counter, which can be programmed in the range 3 to 2047, and a fixed divide by two stage.

$$R = \frac{fosc}{2 \times fcomp}$$

where *fosc* = oscillator frequency,
fcomp = comparison frequency,
R = 'R' counter ratio

For example, where the crystal frequency = 10MHz and a channel spacing comparison frequency of 12·5kHz is required,

$$R = \frac{10^7}{2 \times 12{\cdot}5 \times 10^3} = 400$$

Thus, the 'R' register would be programmed to 400 expressed in binary. The total division ratio would then be 2×400 = 800 since the total division ratio of the 'R' counter plus the ÷2 stage is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage controlled oscillator (VCO) will depend on the division ratios of the 'M' and 'A' counters, the ratio of the external two-modulus prescaler (*P*/*P*+*1*)and the comparison frequency .

The division ratio $N = MP+A$,
where *M* is the ratio of the M counter in the range 3 to 1023 and *A* is the ratio of the 'A' counter in the range 1 to 127.

Note that $M \geqslant A$ and

$$N = \frac{fvco}{fcomp}$$

For example, if the desired VCO frequency = 275MHz, the comparison frequency is 12·5kHz and a two-modulus prescaler of ÷64/65 is being used, then

$$N = \frac{275 \times 10^6}{12{\cdot}5 \times 10^3} = 22 \times 10^3$$

Now, $N = MP+A$, which can be rearranged as $N/P = M+A/P$. In our example we have $P = 64$, therefore

$$\frac{22 \times 10^3}{64} = M + \frac{A}{64}$$

such that $M = 343$ and $A/64 = 0.75$.

Now, *M* is programmed to the integer part = 343 and *A* is programmed to the fractional part×64 i.e., $A = 0{\cdot}75 \times 64 = 48$.
NB The minimum ratio *N* that can be used is P^2-P (4032 in our example) for all contiguous channels to be available.

To check: $N = 343 \times 64 + 48 = 22000$, which is the required division ratio and is greater than 4032 ($= P^2-P$).

When re-programming, the counters are changed only at the zero state. There is no reset to zero, which means that the synthesiser loop lock up time will be variable with respect to the programming sequence timing. When only small changes in frequency are required, the NJ88C28 non-resettable synthesiser should achieve the shortest loop lock up times.

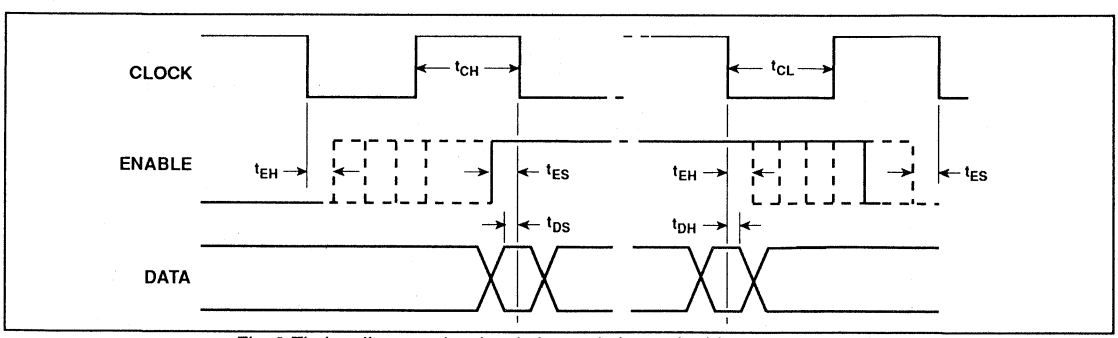


Fig. 3 Timing diagram showing timing periods required for correct operation

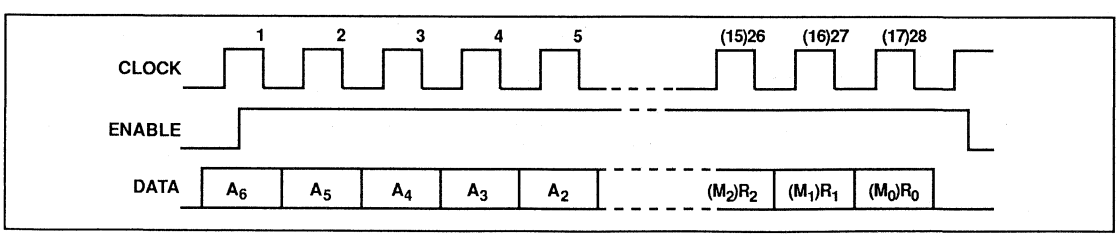


Fig. 4 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain:

$$\frac{K_{PD}\,K_{VCO}}{N}$$

where K_{PD} is the phase detector constant (volts/rad), K_{VCO} is the VCO constant (rad/sec-volt) and N is the overall loop division ratio. When N is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase comparator in the NJ88C28 has a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output, PDB, provides a 'coarse' error signal to enable fast switching between channels.

The PDB output is active until the phase error is within the sample and hold phase detector window, when PDB becomes high impedance. Phase-lock is indicated at this point by a low level on $\overline{LD}$. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock. An internally generated ramp, controlled by the digital output from both the reference and main divider chains, is sampled at the reference frequency to give the 'fine' error signal, PDA. When in phase lock, this output would be typically at the bias voltage set by the external loop filter amplifier; any offset from this would be proportional to phase error.

The relationship between this offset and the phase error is the phase comparator gain, K_{PDA}, which is programmable with an external resistor, RB, and a capacitor, CAP. An internal 50pF capacitor is used in the sample and hold comparator. Typically, the gain is given by:

$$K_{PDA} = \frac{\alpha I_{RB}}{2\pi\, C_{CAP} f_{comp}}$$

where C_{CAP} = internal 50pF + C_{EXT}. Application Note AN112 deals with this further.

A hold capacitor (CH) of non-critical value, which might be typically 470pF, is connected from pin 18 to V_{SS}. A smaller value is sufficient if the required sideband performance is not high. The output from the sample and hold phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO. The PDB gain is:

$$K_{PDB} = \frac{V_{DD}}{4\pi}$$

The stated minimum of 3 for the 'M' counter is true for the PDB output only. To avoid race conditions in the internal phase comparator counter for controlling the PDA timing, the minimum division ratio for the 'M' counter should be 8 or more. Fig. 6 shows a typical NJ88C28 application.

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the inclusion of a resistor between pin 10 (OSC OUT) and the other components, as shown in Fig. 5. A value of between 220Ω and 2·2kΩ is advised, depending on the crystal series resistance.

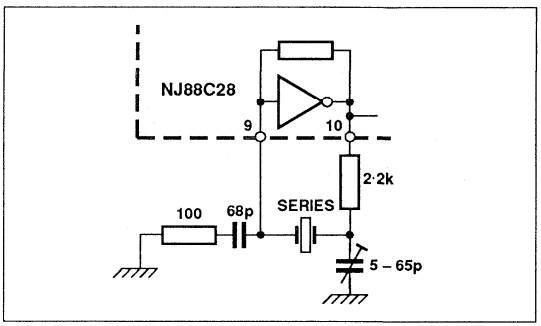


Fig. 5 Suggested crystal oscillator circuit

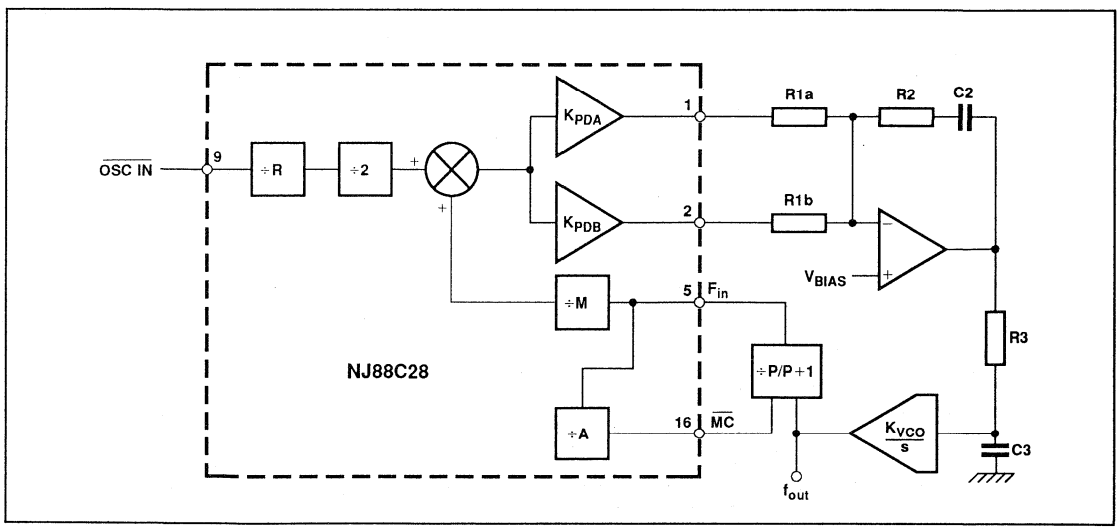


Fig.6 NJ88C28 application circuit

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise latch-up may occur. When programming the device, DATA, ENABLE and CLOCK pins must not exceed V_{DD} as lock up times may be compromised. A suggested interface to prevent this situation is shown in Fig. 7.

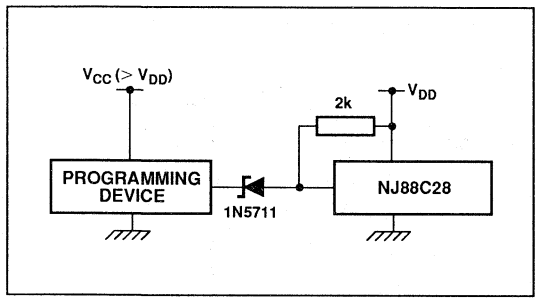


Fig. 7 Suggested programming circuit

LOOP EQUATIONS

$$\omega_0 = \left[\frac{K_{VCO}\,K_{PD}}{N\,\mathbf{R}\,C_2\,C_3\,R_3}\right]^{\frac{1}{3}}$$

$$\zeta = \left[(K_{VCO}\,K_{PD}\,R_2)\,/\,\{(NC_3\,R_3\,\omega_0{}^2)-1\}\right]/\,2\mathbf{R}$$

$$C_3R_3 = \left[\omega_o\,(2\zeta+\mathbf{R})\right]^{-1}$$

$$R_2 = \frac{N\,\omega_0\,(1+2\zeta\mathbf{R})}{K_{VCO}\,K_{PD}\,(\mathbf{R}+2\zeta)}$$

$$C_2 = \frac{K_{VCO}\,K_{PD}\,(2\zeta+\mathbf{R})}{N\,\mathbf{R}\,\omega_0{}^2}$$

where ω_0 = loop natural frequency
ζ = damping factor
$\mathbf{R}$ = ratio of real pole to ω_0
$N = MP+A$
$K_{PD} = K_{PDA}/R_{1a}$
or $K_{PD} = K_{PDB}/R_{1b}$
provided $R_{1a} \gg R_{1b}$

$$\text{PDA window} = \frac{V_{DD}-\left[(V_{T+})+(V_{T-})\right]\,N\,f_{comp}}{2\pi\,K_{PDA}}$$

Further details are to be found in Application Note AN112.

DS3281-1.1

NJ88C30

VHF SYNTHESISER

The NJ88C30 contains all the logic needed for a VHF PLL synthesiser and is fabricated on the GPS high performance, small geometry CMOS process. The circuit contains a reference oscillator and divider, a two-modulus prescaler and 4-bit control register, a 12-bit programmable divider, a phase comparator and the necessary data input and control logic.

FEATURES

- Low Power CMOS
- Easy to Use
- Low Cost
- Single Chip Synthesiser to VHF
- Lock Detect Output

APPLICATIONS

- Mobile Radios
- Hand Held Portable Radios
- Sonobuoys

ORDERING INFORMATION

NJ88C30 KA DP Plastic DIL Package
NJ88C30 KA MP Miniature Plastic DIL Package

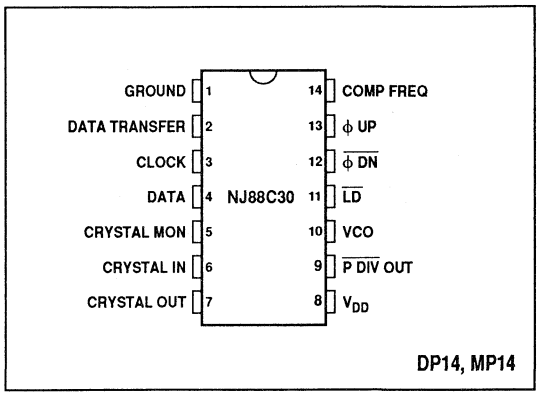


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	−0·3V to 6V
Voltage on any pin	−0·3V to V_{DD}+0·3V
Operating temperature	−30°C to +70°C
Storage temperature	−55°C to +125°C

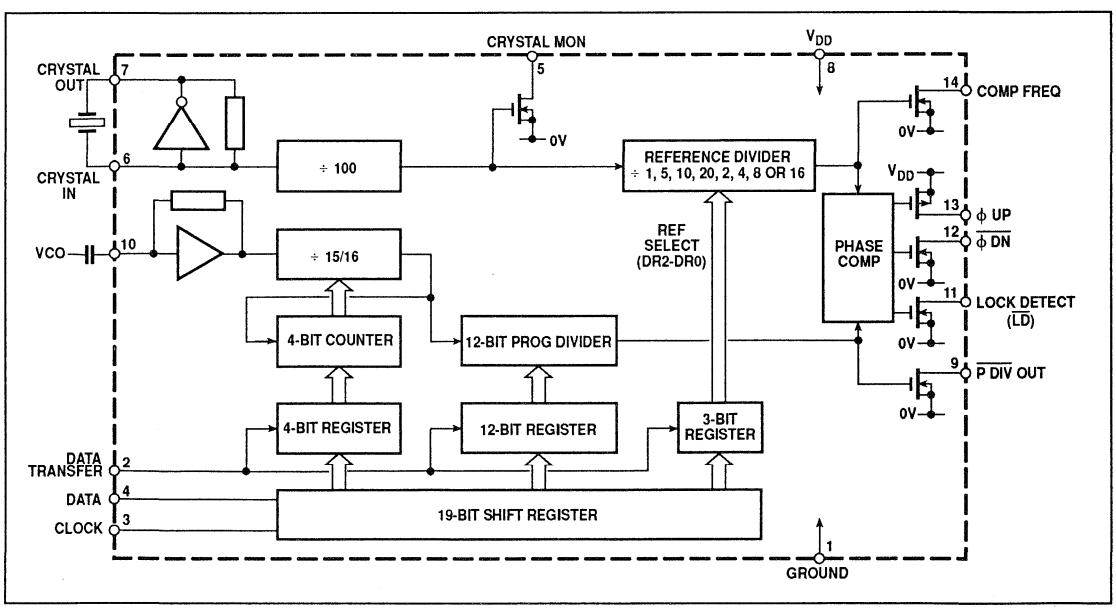


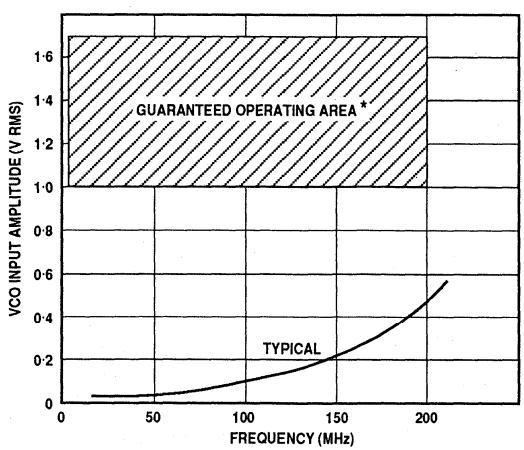
Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{AMB} = −30°C to +70°C, V_{DD} = 5V ±0·5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		4	7	mA	1VRMS VCO input at 200MHz and f_{XTAL} = 10MHz
Crystal Oscillator						
Frequency	6, 7		10	15	MHz	Parallel resonant, fundamental crystal
External input level	6	1			Vrms	AC coupled
High level	6	V_{DD}−1			V	DC coupled
Low level	6			1	V	DC coupled
VCO Input						
Input sensitivity	10	1			Vrms	At 200MHz, see Fig. 3
Slew rate	10	4			V/µs	
Input impedance	10		5pF// 10k			
DATA, DATA TRANSFER and CLOCK Inputs						
High level	2, 3, 4	V_{DD}−1			V	
Low level	2. 3, 4			1	V	
Rise, fall time	2, 3			200	ns	
Data set-up time	3, 4	200			ns	See Fig. 4
Clock frequency	3			2	MHz	
Transfer pulse width	2	500			ns	
CRYSTAL MONITOR Output						
Current sink	5	0·8			mA	V_{OUT} = 0·5V
COMP FREQ, $\overline{LD}$, $\overline{P\ DIV}$						
Current sink	9, 11, 14	1·6			mA	V_{OUT} = 0·5V
ϕ UP / $\overline{\phi}$ $\overline{DN}$						
Current sink	12	0·8			mA	V_{OUT} = 0·5V
Current source	13	0·8			mA	V_{OUT} = V_{DD}−0·5V



* Tested as specified in Table of Electrical Characteristics

Fig. 3 Input sensitivity

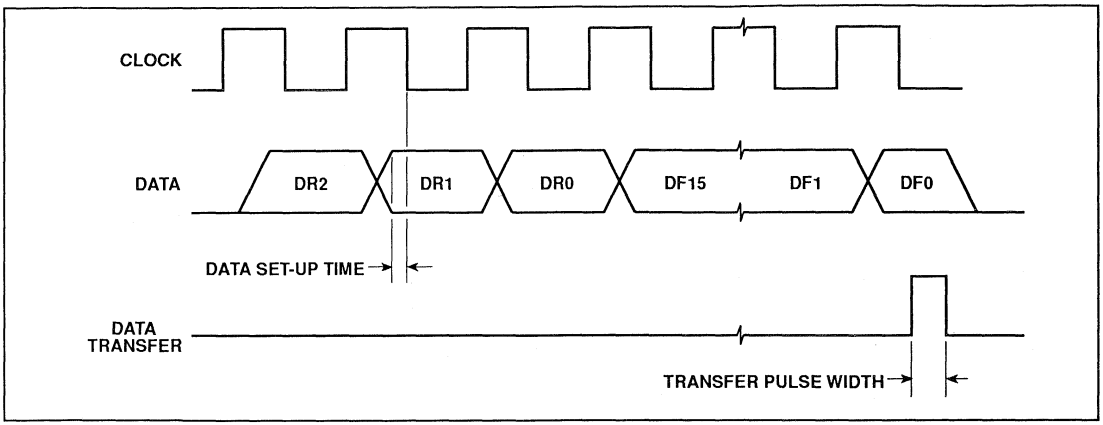


Fig. 4 Input data timing diagram

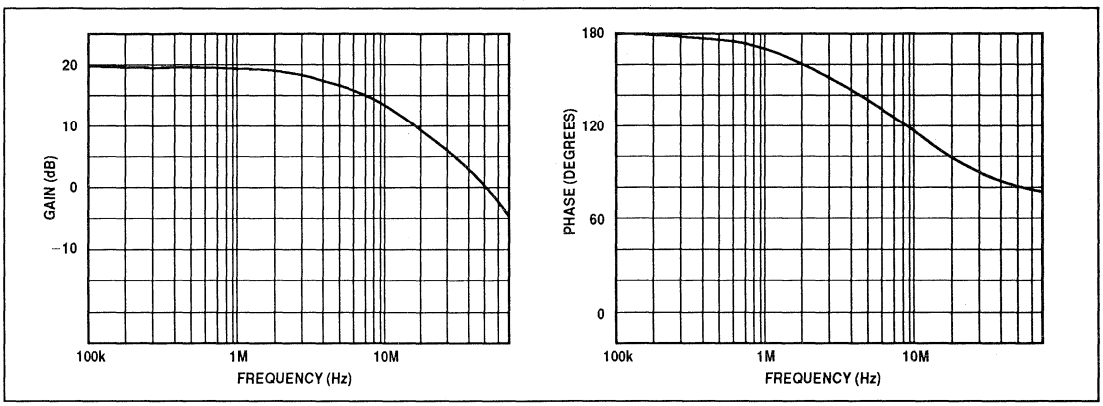


Fig. 5 Gain and phase characteristics of reference oscillator inverter

CIRCUIT DESCRIPTION

Crystal Oscillator and Reference Divider

The Reference oscillator consists of a Pierce type oscillator intended for use with a parallel resonant fundamental crystal. Typical gain and phase characteristics for the oscillator inverter are shown in Fig 5. An external reference oscillator may be used by either capacitively coupling a 1V RMS sinewave into CRYSTAL IN (pin 6) or, if CMOS levels are available, by direct connection to CRYSTAL IN.

The reference oscillator drives a ÷100 prescaler followed by a reference divider to provide a range of comparison frequencies which are selected by decoding the first three bits (DR2, DR1, DR0) of the input data. The possible division ratios and the comparison frequencies (channel spacing) if a 10MHz crystal is used are shown in Table 1.

DR2	DR1	DR0	Total division ratio	Comparison frequency for 10MHz Ref. Osc.
0	0	0	1600	6·25kHz
0	0	1	800	12·5kHz
0	1	0	400	25kHz
0	1	1	200	50kHz
1	0	0	2000	5kHz
1	0	1	1000	10kHz
1	1	0	500	20kHz
1	1	1	100	100kHz

Table 1 Reference divider division ratios

To assist in trimming the crystal, an open drain output at one hundredth of the reference oscillator frequency is provided on CRYSTAL MONITOR pin 5

Programmable Divider

The programmable divider consists of a ÷15/16 two modulus prescaler with a 4-bit control register, followed by a 12-bit programmable divider. A 1V RMS sinewave should be capacitively coupled from the VCO to the divider input VCO pin (pin 10).

The overall division ratio is selected by a single 16-bit word (DF15 to DF0), loaded through the serial data bus. A lower limit of 240 ensures correct prescaler operation; the upper limit is 65535. The VCO frequency in a locked system will be this division ratio multiplied by the comparison frequency.

Phase Comparator

The phase comparator consists of a digital type phase comparator with open drain ϕ UP and ϕ DN outputs and an open drain LOCK DETECT ($\overline{LD}$) output. Open drain outputs from the reference divider and programmable divider are provided for monitoring purposes or for use with an external phase comparator. Waveforms for all these outputs are shown in Fig.6. The duty cycle of ϕ UP and ϕ DN versus phase difference are shown in Fig. 7. The phase comparator is linear over a $\pm 2\pi$ range and if the phase gains or slips by more than 2π, the phase comparator outputs repeat with a 2π period.

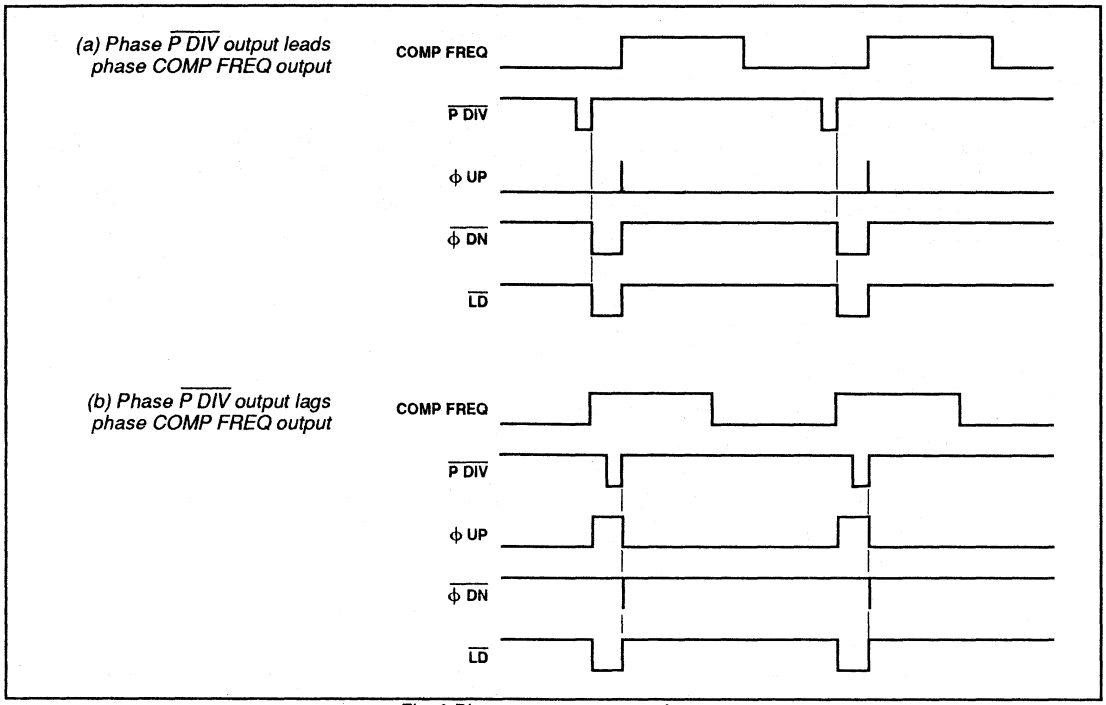


Fig. 6 Phase comparator waveforms

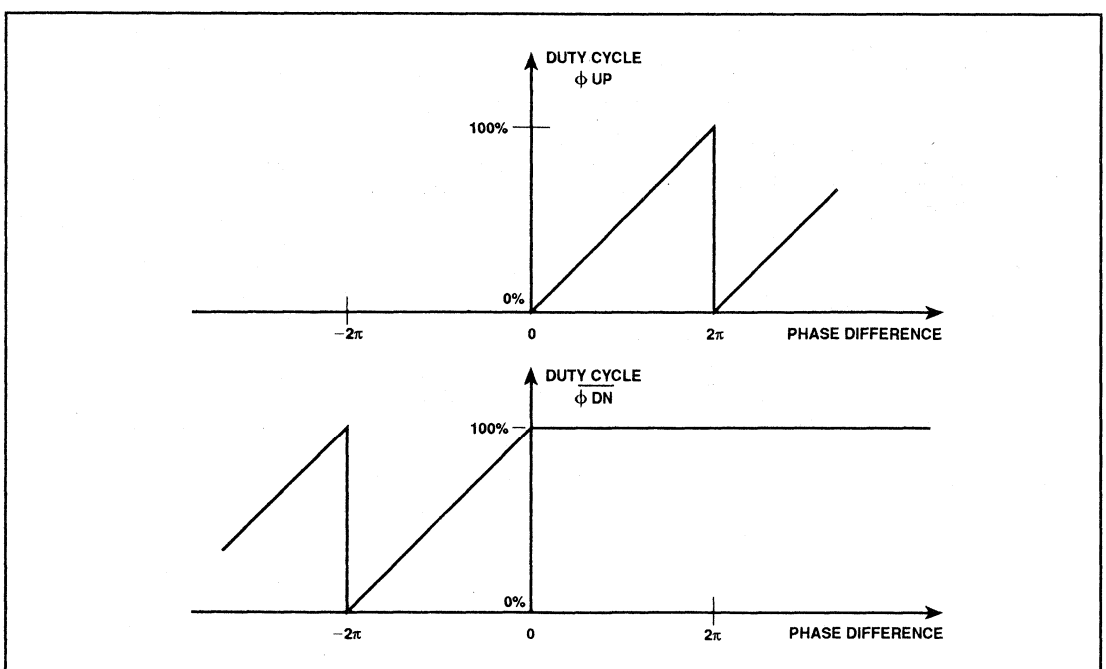


Fig. 7 Phase comparator output characteristics

Once the phase difference exceeds 2π, the comparator will gain or slip one cycle and then try to lock on to the new zero phase difference. Note that very narrow pulses may be seen on the inactive phase comparator output at the end of the pulse on the active output, as shown in Fig. 6.

Data Input and Control Register

To control the synthesiser a simple three-line serial input is used with DATA, CLOCK and DATA TRANSFER signals. The data consists of 19 bits; the first three, DR2, DR1 and DR0, control the reference divider while the following sixteen, DF15 to DF0, control the prescaler and programmable divider. Until the synthesiser receives the DATA TRANSFER pulse, it will use the previously loaded data; on receiving the pulse it will switch rapidly to the new data.

APPLICATIONS

A simplified circuit for a synthesiser intended for VHF broadcast receiver applications is shown in Fig. 8. When the varicap line drive voltage necessary to tune the required band is greater than 5V, some form of level shifter such as the operational amplifier shown in Fig. 8 is required.

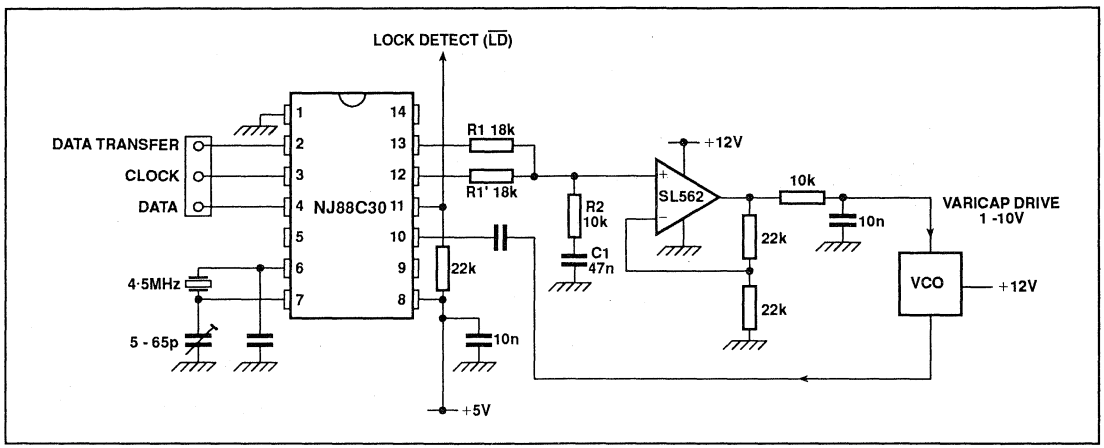


Fig.8. Typical application

PROGRAMMING EXAMPLE

1.Maximum Frequency

For a channel spacing (comparison frequency, f_{comp}) of 5kHz when using a 10MHz crystal oscillator, the reference divider ratio will need to be 2000 (seeTable 1) This is programmed as binary 100 (= 4_{HEX}) in the most significant three of the 19 bits (MSB programmed first).

To obtain the maximum VCO frequency of 200MHz the programmable divider ratio would be:

$$\frac{200\times10^6}{5\times10^3} = 40\times10^3 \text{ which is } 9C40_{HEX}$$

The program word would then be as shown in Table 2.

	DR			DF															
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0
Hex	4			9				C				4				0			

Table 2 Maximum VCO frequency programming (f_{XTAL} = 10MHz, f_{comp} = 5kHz)

2. Minimum Frequency

Using the same crystal frequency and channel spacing (10MHz, 5kHz), the lower limit of programmable divider ratio of 240 = $F0_{HEX}$ gives a minimum programmable VCO frequency of $240\times5\times10^3$ = 1·2MHz. The program word for this frequency is therefore as shown in Table 3.

	DR			DF															
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
Hex	4			0				0				F				0			

Table 3 MinimumVCO frequency programming (f_{XTAL} = 10MHz, f_{comp} = 5kHz)

DS 2429 3.2

NJ88C33

FREQUENCY SYNTHESISER (I²C BUS PROGRAMMABLE) WITH CURRENT SOURCE PHASE DETECTOR OUTPUTS

(Supersedes September 1991 edition)

The NJ88C33 is a synthesiser circuit fabricated on GPS's 1.4 micron CMOS process, assuring very high performance. It is I²C compatible and can also be programmed at up to 5MHz. It contains a 16-bit R counter, a 12-bit N counter and a 7-bit A counter.

A digital phase comparator gives improved loop stability with current source outputs to reduce loop components. A voltage doubler is provided for the loop driver to improve control voltage range to the VCO when operating at low supply voltages.

FEATURES

- Easy to Use
- Low Power Consumption (15 mW)
- Single Supply 2.5V to 5.5V
- Digital Phase Comparator with Current Source Outputs
- Serial (I²C Compatible) Programming, 5MHz max;
- Channel Loading in 8μs
- 150MHz Input Frequency Without Prescaler at 4.5V (52MHz at 2.7V)
- Standby Modes
- Use of Two-Modulus Prescaler is Possible

APPLICATIONS

- Cordless Telephones (CT2, DECT)
- Cellular Telephones (GSM, PCN, ETACS)
- Hand Held Marine Radios
- Sonarbuoys
- Video Clock generators

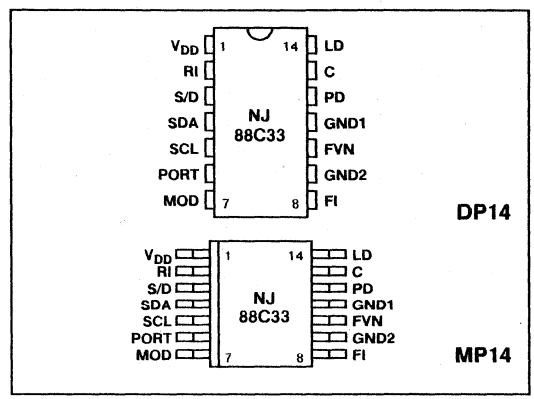


Fig.1 Pin connections (not to scale) - top views

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	-0.3V to 7V
Input voltage, V_{IM1}	-0.3V to V_{DD} + 0.3V
Output voltage on pin 13, V_{IM2}	-V_{DD} to 0V
Storage temperature, T_{stg}	-55°C to + 125°C

ORDERING INFORMATION

NJ88C33 MA DP (Industrial - Plastic DIL package)
NJ88C33 MA MP (Industrial - Miniature Plastic DIL package)

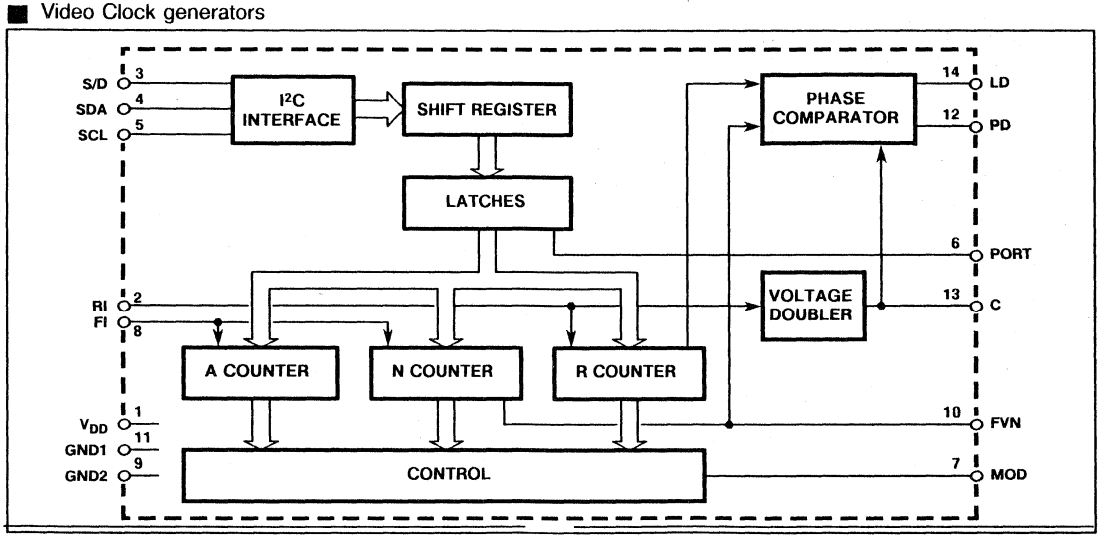


Fig.2 Simplified block diagram of NJ88C33

PIN DESIGNATIONS

Pin No.	Pin Name	Description
1	V_{DD}	Supply voltage (normally 5V or 3V).
2	RI	Reference frequency input from an accurate source, normally a crystal oscillator. The input is normally an AC coupled sinewave but may be a DC coupled square wave.
3	S/D	Single/dual modulus operating mode selection input. Single modulus operation is selected by driving the pin low. 'High' selects dual modulus mode.
4	SDA	I²C bus data input pin. It is also an open-drain output for generating I²C bus acknowledge pulses.
5	SCL	I²C bus clock input. It can be clocked at up to 5MHz.
6	PORT	Output control pin, which can be programmed via the I²C bus. It can be connected to the S/D pin to select single or dual modulus mode under bus control.
7	MOD	Modulus control pin. It is high in single modulus mode but switches in dual modulus operation. In dual modulus mode, MOD remains low during operation of the A counter until A = 0; MOD then remains high until N = 0, when both counters are reloaded. It can be programmed via the I²C bus as an open-drain or push-pull output.
8	FI	Frequency input from a VCO or prescaler. The input is normally an AC coupled sinewave but may be a DC coupled square wave.
9	GND2	Dedicated ground for the FI input buffer. It should be connected to the VCO ground or the prescaler ground, if used. Any noise on this pin will affect the performance of the VCO loop.
10	FVN	Open-drain output from the N counter.
11	GND1	Ground supply pin (global).
12	PD	Tristate current output from the phase detector. The polarity of the output can be programmed via the I²C bus.
13	C	Voltage doubler output. The operation of the doubler can be controlled via the I²C bus. In applications where the voltage doubler is switched off, this pin should be connected to GND1; a reservoir capacitor should be connected from this pin to GND1 for applications where it is switched on.
14	LD	Open-drain lock detect output - requires integration if used.

OPERATING RANGE

Test conditions (unless otherwise stated):
PLL locked, RI = 10MHz

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	2.5	5	5.5	V	
Ambient temperature	T_{amb}	-40		+85	°C	
Supply current						
Single modulus	I_{DD}		2.1	3.0	mA	FI = 50MHz, V_{FI} = 150mVrms, N,R > 1000 without voltage doubler, V_{DD} = 5V, T_{amb} = 25°C
Dual modulus	I_{DD}		2	3.0	mA	FI = 10MHz, V_{FI} = 500mVrms, N,R > 1000 without voltage doubler, V_{DD} = 5V, T_{amb} = 25°C
Standby mode	I_{DD}			1	μA	FI = 50MHz, V_{FI} = 150mVrms, preamp off, divider off, V_{DD} = 5V, T_{amb} = 25°C
Standby mode	I_{DD}		1.0	1.5	mA	FI = 50MHz, V_{FI} = 150mVrms, preamp on, divider off, V_{DD} = 5V, T_{amb} = 25°C

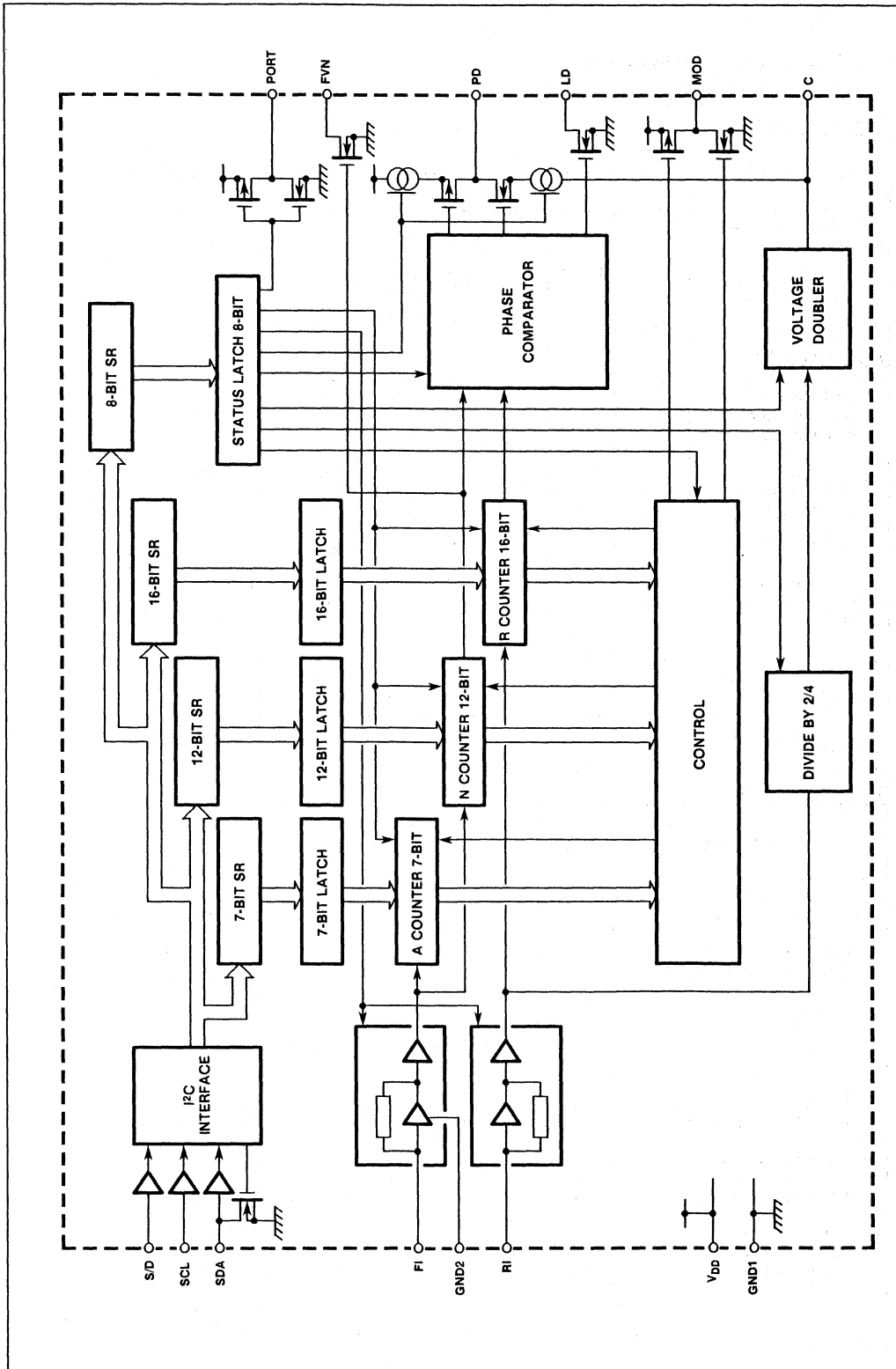


Fig.3 Functional block diagram

ELECTRICAL CHARACTERISTICS

Operating conditions (unless otherwise stated):
V_{DD} = 4.5V to 5.5V, T_{amb} = -40°C to +85°C

INPUT SIGNALS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input Signals SDA, SCL, S/D						
Input voltage high	V_{IH}	$0.7V_{DD}$		V_{DD}	V	
Input voltage low	V_{IL}	0		$0.3V_{DD}$	V	
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	µA	$V_{IN} = V_{DD} = 5.5V$
Input Signal RI						
Input frequency	f_{max}			52	MHz	Sinewave input
Input voltage	V_{Irms}	100			mV	Note 1, 2
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	µA	$V_{IN} = V_{DD} = 5.5V$
Input Signal FI						Dual modulus operation
Input frequency	f_{max}			52	MHz	Sinewave input
Input voltage	V_{Irms}	50			mV	Note 1, 2
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	µA	$V_{IN} = V_{DD} = 5.5V$
Input Signal FI						Single modulus operation
Input frequency	f_{max}			150	MHz	Sinewave input
Input voltage	V_{Irms}	30			mV	FI = 0-70MHz Note 1, 2
	V_{Irms}	100			mV	FI = 70-120MHz Note 1, 2
	V_{Irms}	200			mV	FI = 120-150MHz Note 1, 2
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	µA	$V_{IN} = V_{DD} = 5.5V$

Note. 1 Lowest noise floor achieved at 10dB above this level with I²C bus operating. The source impedance should be less than 2kΩ.
Note. 2 DC coupled input amplitude $V_{IRMS} > 0.8\ V_{DD}$.

OUTPUT SIGNALS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output Signals SDA, LD						
Output voltage low	V_{OL}			0.4	V	Open drain, I_{OL} = 3mA
Output Signal PD						C_L = 400pF, tristate output
High current mode (see Fig.4)	I_{HU}	1.9	2.5	3.1	mA	$0 < V_{PD} < 4.5$, V_{DD} = 5V, T = 25°C Note 1
	I_{HD}	-1.9	-2.5	-3.1	mA	$0.4 < V_{PD} < 5$, V_{DD} = 5V, T = 25°C Note 1
Low current mode	I_{LU}	0.475	0.625	0.775	mA	$0 < V_{PD} < 4.6$, V_{DD} = 5V, T = 25°C Note 1
	I_{LD}	-0.475	-0.625	-0.775	mA	$0.4 < V_{PD} < 5$, V_{DD} = 5V, T = 25°C Note 1
Tristate	I_Z		50		nA	T_{amb} = -25°C to +60°C
Output Signal FVN						Open drain output
Output voltage low	V_{OL}			0.4	V	I_{OL} = 1mA
Output low pulse width	t_{WL}			1/FI		C_L = 30pF
Output Signals MOD, PORT						Push-pull output
Output voltage high	V_{OH}	V_{DD}-0.4			V	I_{OH} = 0.5mA
Output voltage low	V_{OL}			0.4	V	I_{OL} = 0.5mA
Output Signal LD						Open drain output
Output voltage low	V_{OL}			0.4	V	I_{OL} = 3mA, CL = 30pF
Output low pulse width	t_{WL}		10	1/FVN	ns	Loop locked
				$1/f_C$		Loop not locked
						FVN = FI/N
						f_C = RI/R

Note 1 Temperature coefficient for current is typically -0.7%/°C

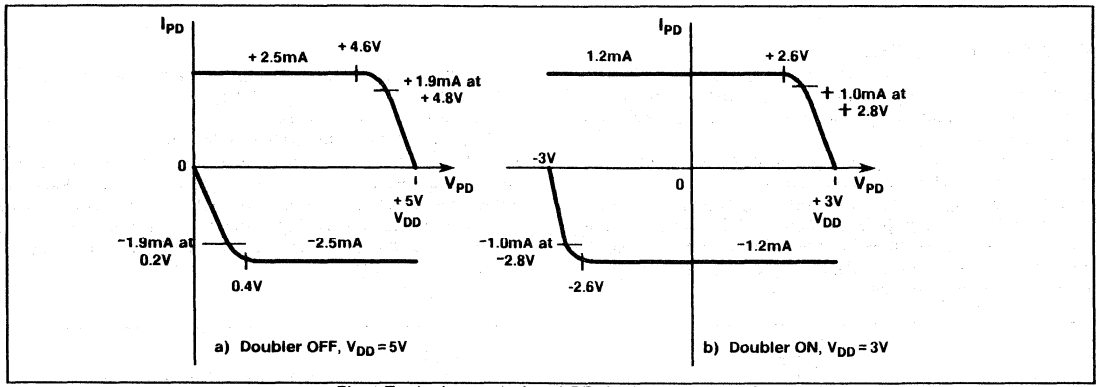


Fig.4 Typical output signal PD, high current mode

VOLTAGE DOUBLER $V_{DD} \leq 3V$

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output Pin C						
Output voltage	V_C	$-V_{DD}$		$-V_{DD}+0.8V$	V	f_{VD} = 2MHz, I_{OC} = 0μA, V_{DD} = 3V
	V_C	$-V_{DD}$		$-V_{DD}+1.5V$	V	f_{VD} = 2MHz, I_{OC} = 100μA, V_{DD} = 3V
Current Consumption	I_D			100	μA	f_{VD} = 2MHz, I_{OC} = 0μA, V_{DD} = 3V

TIMING INFORMATION

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input Signal RI						
Input frequency	f_{max}	0		52	MHz	
Input frequency	f_{max}	0		10	MHz	V_{DD} = 2.7V
Rise time	t_R			1.5	μs	
Fall time	t_F			1.5	μs	
Slew rate		3			V/μs	
Input Signal FI						Dual modulus
Input frequency	f_{max}	0		52	MHz	
Input frequency	f_{max}	0		20	MHz	V_{DD} = 2.7V
Rise time	t_R			1.5	μs	
Fall time	t_F			1.5	μs	
Slew rate		3			V/μs	
Input Signal FI						Single modulus
Input frequency	f_{max}			150	MHz	
Input frequency	f_{max}	0		52	MHz	V_{DD} = 2.7V
Rise time	t_R	0		1.5	μs	
Fall time	t_F			1.5	μs	
Slew rate		3			V/μs	
Output Signal PORT						
Rise time	t_R			1	μs	C_L = 30pF
Fall time	t_F			1	μs	C_L = 30pF
Output Signal FVN						
Fall time	t_F		20		ns	C_L = 30pF
Output Signal MOD						
Rise time	t_R			10	ns	C_L = 30pF
Fall time	t_F			10	ns	C_L = 30pF
Delay time (L→H)	t_{DLH}			15	ns	C_L = 30pF Measured from +Ve edge of FI
Delay time (H→L)	t_{DHL}			15	ns	C_L = 30pF Measured from +Ve edge of FI

PHASE COMPARATOR

The phase comparator produces current pulses of duration equal to the difference in phase between the comparison frequency (f_C = RI/R), and f_{VN}, the divided-down VCO frequency (FI/N).

When status bit 4 is set high the positive polarity mode of the output PD is selected. When f_C leads f_{VN} the PD output goes high; when f_{VN} leads f_C it goes low. Similarly, selecting the negative polarity mode of PD by programming bit 4 of the status register low causes PD to have the inverse polarity. The loop filter integrates the current pulses to produce a voltage drive to the VCO.

No pulses are produced when locked. The lock detect output, LD, produces a logic '0' pulse equal to the phase difference between f_C and f_{VN}.

When the phase difference between fc and f_{VN} is too small to be resolved by the phase detector then no current pulses are produced. In this region the loop does not reduce the close-in noise on the VCO output. This can be overcome using a very high value resistor to leak a few nanoAmps of current from the filter and keep the loop on the edge of the region.

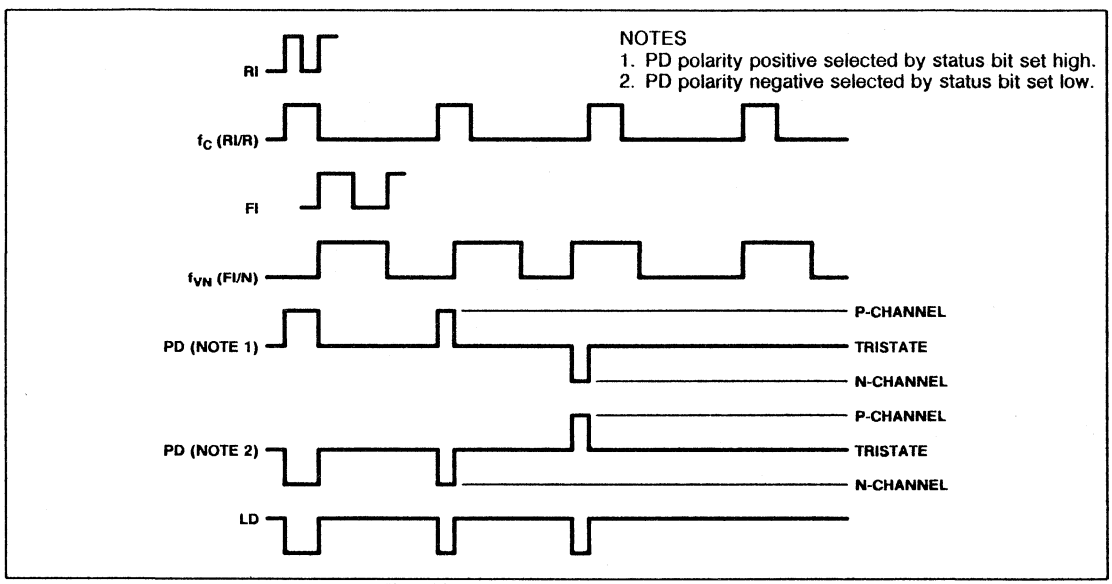


Fig.5 Phase comparator phase diagram

PROGRAMMING

Transmission Protocol

I²C programming messages consist of an address byte followed by a sub-address byte followed by 1, 2 or 3 bytes of data. Bit 7 of the address byte must match the setting of the S/D pin for the address to be recognised. This allows for separate addressing of two NJ88C33 synthesisers on the same bus. The sub-address should be set to select the correct registers to be programmed and should be followed by the appropriate number of data bytes. Registers are not programmed until the complete message protocol has been checked.

Each message should commence with a START condition and end with a STOP condition unless followed immediately by another transfer, when the STOP condition may be omitted.

Data is transferred from the shift register to the latches on a STOP condition or by a second START condition.

A START condition is indicated by a falling edge on the Serial Data line, SDA, when the Serial Clock line, SCL, is high.

A rising edge on SDA when SCL is high indicates a STOP condition as shown in Fig.6.

Data on SDA is clocked into the NJ88C33 on the rising edge of SCL. The NJ88C33 acknowledges each byte transferred to it by pulling the SDA line low for one cycle of SCL after the last bit has been received.

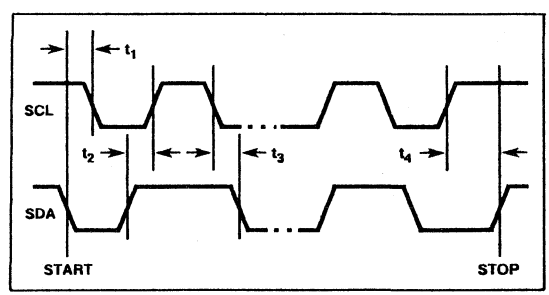


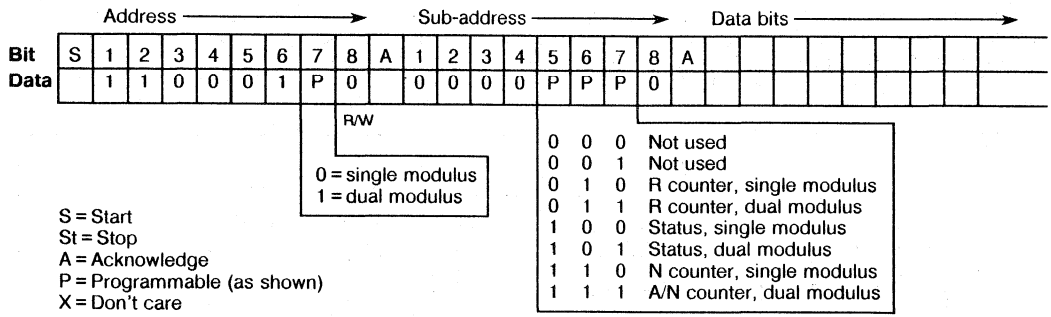
Fig.6 I²C timing diagram

I²C TIMING INFORMATION
VDD = 4.5V to 5.5V, Tamb = -40°C to +85°C

Parameter	Symbol	Value		Unit
		Min.	Max.	
Serial clock frequency	f_{SCL}		5	MHz
SCL hold after START	t_1	20		ns
Data set-up time	t_2	20		ns
Data hold after SCL low	t_3	0		ns
SCL set-up before STOP	t_4	20		ns

Address and Sub-Address Formats

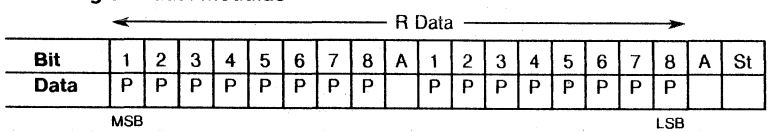
The correct addressing sequence for the NJ88C33 is shown below. The START condition is followed by the address byte, the acknowledge from the NJ88C33, the sub-address byte, another acknowledge then the associated data. The correct values for each address and sub-address are listed, together with the message selection options.



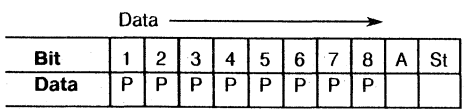
Data Formats

Each of the data formats should be preceded contiguously by the addressing sequence given above.

R counter : single or dual modulus



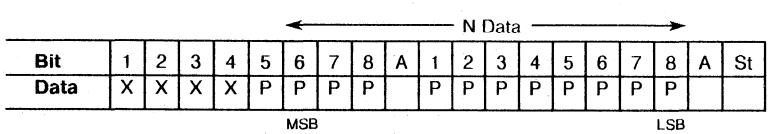
Status : single or dual modulus



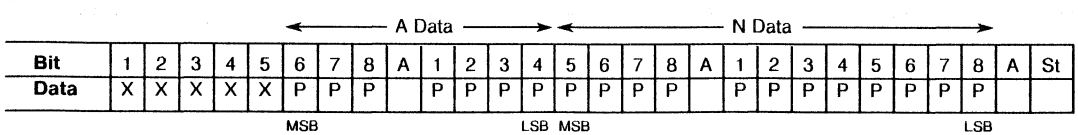
Status Byte		
Bit	**0**	**1**
1	PORT = low	PORT = high
2	Counters off (1)	Counters on
3	FI and RI off (2)	FI and RI on
4	PD = polarity negative	PD = polarity positive
5	PD bias = 0.625mA	PD bias = 2.5mA
6	f_{VD} = RI/2	f_{VD} = RI/4
7	Doubler off	Doubler on (3)
8	MOD = push-pull	MOD = open drain

NOTES
1. In this standby mode the counters are disabled but the voltage doubler and I²C interface can both function.
2. In this standby mode the FI and RI preamplifiers are disabled, which stops the counters and the voltage doubler. The I²C interface still operates.
3. The voltage doubler should only be used when $V_{DD} \leq 3.0V$

N counter : single modulus



A/N counters : dual modulus



APPLICATION CIRCUITS

Single Modulus

In this mode, the NJ88C33 synthesiser can be used with or without a fixed modulus prescaler. The R counter is programmed with a value to produce a comparison frequency f_C. When the N counter is changed by 1 the loop is no longer in lock and the phase detector output produces current pulses to bring the loop back into lock. These pulses are integrated by the loop filter to produce the VCO voltage drive. When the VCO loop is locked, $FI/N = f_C$ i.e., the VCO frequency is $N \times f_C$.

Using a prescaler with a division ratio P, the smallest VCO output frequency step is Pf_C and the VCO frequency is PNf_C.

If a low pass filter is connected to the lock detect output as shown and sampled by the microprocessor, the proximity of the synthesiser loop to lock can be evaluated.

The A counter is not used in this mode.

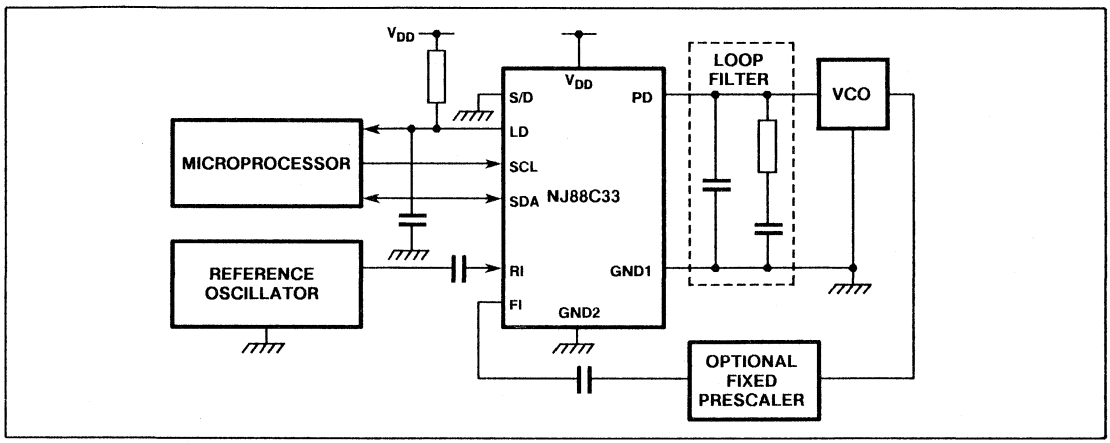


Fig.7 Single modulus application

Dual Modulus

This mode allows much higher frequencies to be used in conjunction with a prescaler but maintains the step size, f_C. In this mode, a dual modulus prescaler (with ratios P and P + 1) must be used with the NJ88C33. The A counter controls the MOD output, which is used to select the division ratio of the prescaler.

When the A counter is non-zero, the MOD output is low and goes high when the A counter has counted down to zero. MOD remains high until the N counter reaches zero, when both counters are re-loaded. Thus, the prescaler divides by P for N-A cycles and by P + 1 for A cycles of FI. The VCO frequency is given by $PNf_C + Af_C$.

Note that programming A = 0 produces a count of 128 cycles.

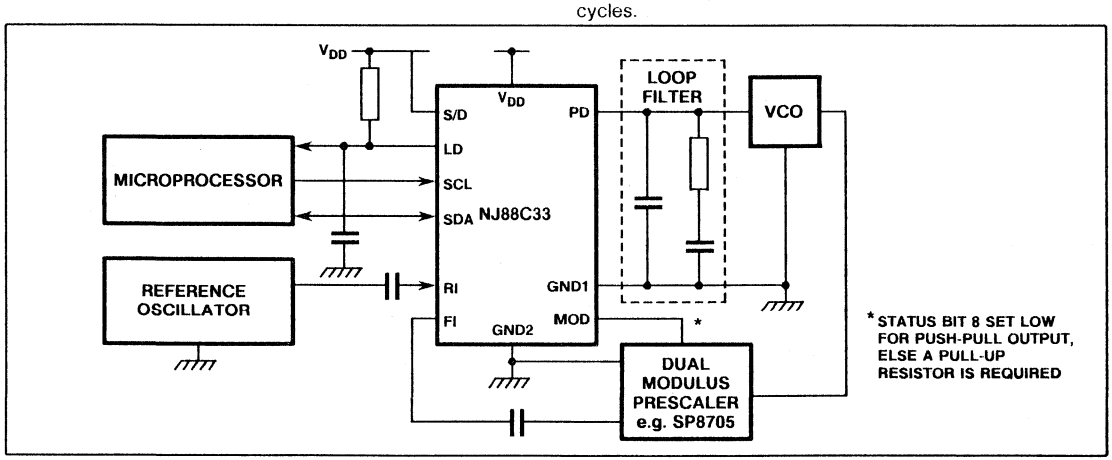


Fig.8 Dual modulus application

VCO Driving Without Voltage Doubler

To switch off the voltage doubler, bit 7 of the status register is programmed low. This will reduce current consumption and minimise noise. The voltage doubler output C should be connected to GND1 as connection to GND2 would induce noise in the VCO loop.

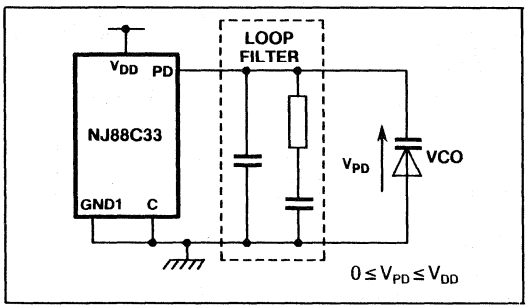


Fig.9 Driving a VCO without voltage doubler

VCO Driving With Voltage Doubler

The voltage doubler is switched on by setting bit 7 of the status register high. It is recommended that a reservoir capacitor of at least 1μF be connected from C to GND1.

The voltage doubler is designed to boost VCO drive in low voltage applications.

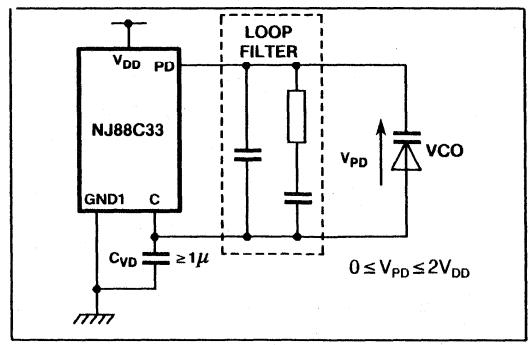


Fig.10 Driving a VCO using the voltage doubler

Further Applications Information

A stand-alone programmer card and an evaluation board are available for evaluating the NJ88C33. The programmer card allows two sets of variables to be programmed into both the divider and status registers during alternate programming cycles, at either the standard I²C bus rate of 100kHz or at 2MHz.

Initialisation is with either a manual push-button or by an external logic level pulse; a synchronisation output is provided to allow a quick assessment of 'step' and 'settle' responses to be made.

The NJ88C33 evaluation board (Fig. 11) demonstrates the preferred layout technique - providing a reference oscillator, a 60 to 80MHz VCO and a simple loop filter to complete a minimal frequency synthesiser loop. The two units allow analysis of different loop variables as well as the selection of comparison frequencies for fast frequency-hopping loops.

Application Note: AN94, *'Using the NJ88C33 PLL Synthesiser'* explains the design equations and demonstrates the use of the device, and is available from your local GPS customer service centre.

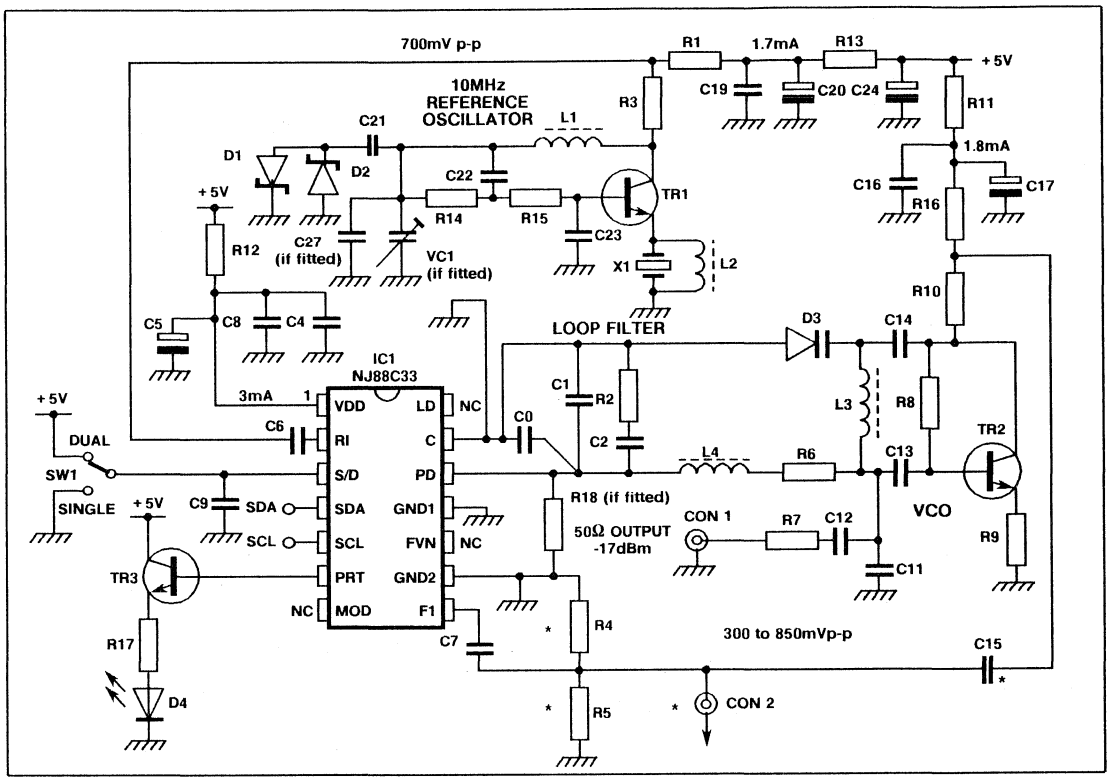


Fig.11 Typical applications circuit

* Insert C15, delete R4 and R5 if CON2 is to be used to monitor the VCO. Delete C15 insert R4 and R5 if CON is to provide an external source, otherwise short C15 and delete R4, R5 and CON2.

COMPONENT LIST FOR FIG.11

Capacitors		Capacitors		Resistors		Inductors		Miscellaneous	
C0	1nF 10%	C17	22µF/35V Elect.	R1	270Ω	L1	15µH 10%	IC1	NJ88C33
C1	100nF 10%	C19	10nF 10%	R2	470Ω	L2	220µH 10%	X1	10.00MHz 5ppm series
C2	1µF Tant.	C20	22µF/35V Elect.	R3	330Ω	L3	180nH 20%	SW1	Miniature slide switch
C4	10nF 10%	C21	10nF 10%	R4	100Ω	L4	470µH 10%	CON1	SMC socket
C5	22µF/35V Elect.	C22	10nF 10%	R5	100Ω			CON2	SMC socket
C6	10nF 10%	C23	22pF 5% NPO	R6	1kΩ	**Diodes**		PCB	C33ISS2
C7	1nF 10%	C24	22µF/35V Elect.	R7	120Ω				
C8	1nF 10%	C27	22pF 5% NPO	R8	27kΩ	D1	1N6263 Schottky		
C9	1nF 10%	VC1	3p5-22p	R9	Link	D2	1N6263 Schottky		
C11	150pF 5% NPO			R10	1kΩ	D3	BBY40 varicap		
C12	1nF 10%			R11	10Ω	D4	5mm red LED		
C13	1nF 10%			R12	10Ω				
C14	2p7 ± 0.5pF NPO			R13	10Ω	**Transistors**			
C15	10nF 10%			R14	22kΩ				
C16	10nF 10%			R15	2.7kΩ	TR1	BFS17 RF NPN		
				R16	330R	TR2	BFS17 RF NPN		
				R17	100Ω	TR3	2N3904 Switching		
				R18	33MΩ				

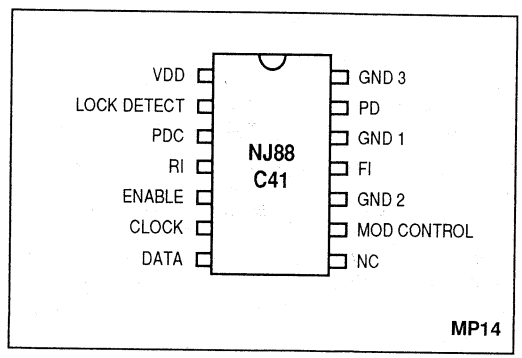
NOTES
1. With the exception of electrolytics, all capacitors are surface mount types
2. All resistors are 0.25W, ±2%
3. C0, C1, C2, C11, C12, C13 and C14 must be low leakage types.
4. R18 may be required to optimise VCO close in noise performance.

DS 3282 -1

NJ88C41

LOW POWER FREQUENCY SYNTHESISER (3 WIRE BUS)

The NJ88C41 is a low power frequency synthesiser device manufactured on GEC Plessey Semiconductors advanced CMOS process. The device is designed to operate as a single chip device, in application upto 250MHz or with a prescaler, such as the SP87xx series, into the GHz range. The device uses switched current source outputs from its phase detector to minimise external components. Programming is via a 3 wire bus. Operation from 2.7 volts upwards is supported.



FEATURES

- Operation with or without prescaler
- Operation upto 250MHz @ 4.5V (100MHz @ 2.7V)
- Low power consumption (25mW @ 250MHz, 4.5V) (10mW. 50MHz. 2.7V)
- Output current programmable upto 2.5mA
- Simple programming interface with quick channel step instruction
- Lock detect pin
- 16 bit reference, 12 bit main, 7 bit auxiliary registers
- Low power stand-by mode

APPLICATIONS

- Cellular radio
- Cordless telephones
- Land mobile and marine radio

GEC PLESSEY
SEMICONDUCTORS

SL560

300MHz LOW NOISE AMPLIFIER

This monolithic integrated circuit contains three very high performance transistors and associated biasing components in an eight-lead TO-5 package forming a 300MHz low noise amplifier. The configuration employed permits maximum flexibility with minimum use of external components. The SL560C is a general purpose low noise, high frequency gain block.

The device is also available as the SL560AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

FEATURES

- Gain up to 40dB
- Noise Figure less than 2dB (Rs 200 ohm)
- Bandwidth 300MHz
- Supply Voltage 2-15V (Depending on Configuration)
- Low Power Consumption

APPLICATIONS

- Radar IF Preamplifiers
- Infra-Red Systems Head Amplifiers
- Amplifiers in Noise Measurement Systems
- Low Power Wideband Amplifiers
- Instrumentation Preamplifiers
- 50 ohm Line Drivers
- Wideband Power Amplifiers
- Wide Dynamic Range IF Amplifiers
- Aerial Preamplifiers for VHF TV and FM Radio

ABSOLUTE MAXIMUM RATINGS

Supply voltage (Pin 4)	+15V
Storage temperature	-55°C to 150°C (CM) -55°C to 125°C (DP)
Junction temperature	150°C (CM) 125°C (DP)
Thermal resistance	
Junction-case	60°C/W (CM)
Junction ambient	220°C/W (CM) 230°C/W (DP)
Maximum power dissipation	See Fig.15
Operating temperature range	-55°C to +125°C (CM) at 100mW -55°C to +100°C (DP) at 100mW

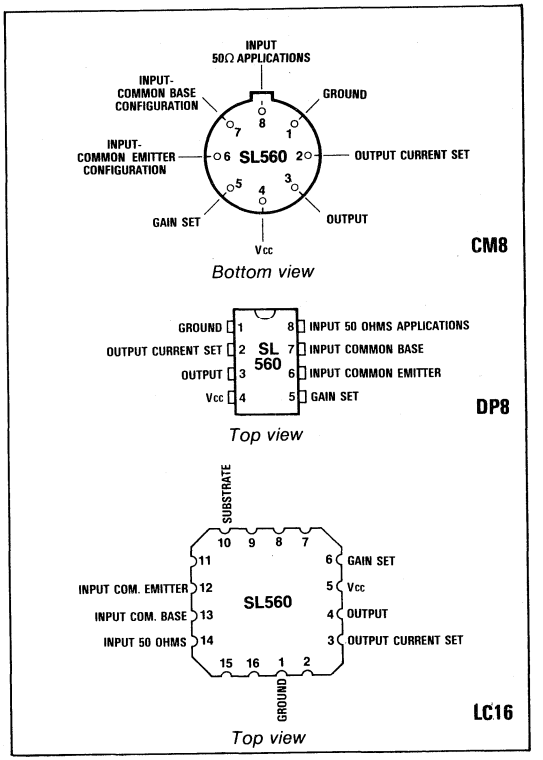


Fig.1 Pin connections

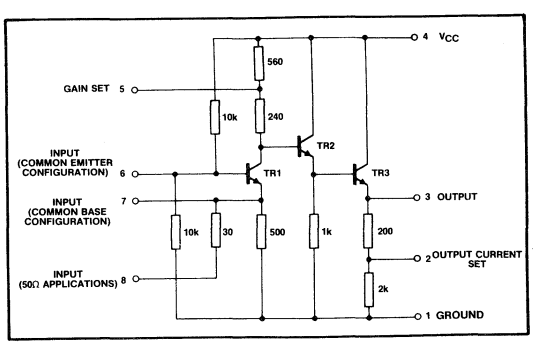


Fig.2 SL560C circuit diagram

ORDERING INFORMATION

SL560 AC CM
SL560 C CM
SL560 C DP
SL560 C LC
SL560 CB CM
SL560 C BSS2 NA CM

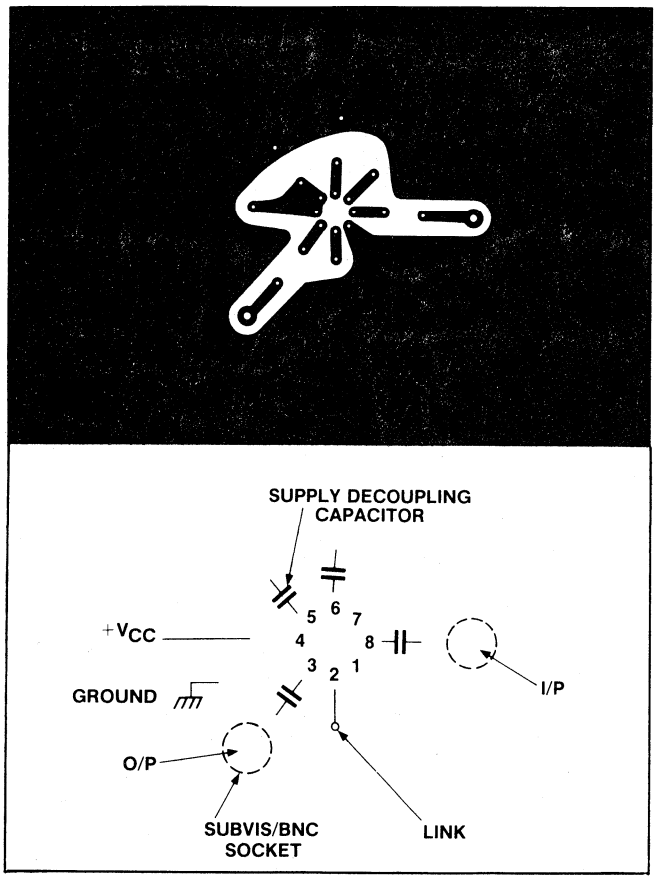


Fig.3 PC layout for 50Ω line driver (see Fig.6)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Frequency = 30MHz; V_{CC} = 6V; R_S = R_L = 50Ω; T_{amb} = 25°C; Test Circuit: Fig.6

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	11	14	17	dB	
Gain flatness		±1.5		dB	10MHz - 220MHz
Upper cut-off frequency		250		MHz	
Output swing	+5	+7		dBm	V_{CC} 6V } See Fig.5
		+11		dBm	V_{CC} = 9V }
Noise figure (common emitter)		1.8		dB	R_S = 200Ω
		3.5		dB	R_S = 50Ω
Supply current		20	30	mA	

CIRCUIT DESCRIPTION

Three high performance transistors of identical geometry are employed. Advanced design and processing techniques enable these devices to combine a low base resistance ($R_{bb'}$) of 17Ω (for low noise operation) with a small physical size - giving a transition frequency, f_T, in excess of 1GHz.

The input transistor (TR1) is normally operated in common base, giving a well defined low input impedance. The full voltage gain is produced by this transistor and the output voltage produced at its collector is buffered by the two emitter followers (TR2 and TR3). To obtain maximum bandwidth the capacitance at the collector of TR1 must be minimised. Hence, to avoid bonding pad and can capacitances, this point is not brought out of the package. The collector load resistance of TR1 is split, the tapping being accessible via pin 5. If required, an external roll-off capacitor can be fixed to this point.

The large number of circuit nodes accessible from the outside of the package affords great flexibility, enabling the operating currents and circuit configuration to be optimised for any application. In particular, the input transistor (TR1) can be operated in common emitter mode by decoupling pin 7 and using 6 as the input. In this configuration, a 2dB noise figure (R_S = 200Ω) can be achieved. This configuration can give a gain of 35dB with a bandwidth of 75MHz (see Figs. 8 and 9) or, using feedback 14dB with a bandwidth of 300MHz (see Figs. 10 and 11).

Because the transistors used in the SL560C exhibit a high value of f_T, care must be taken to avoid high frequency instability. Capacitors of small physical size should be used, the leads of which must be as short as possible to avoid oscillation brought about by stray inductance. The use of a ground plane is recommended.

Further applications information is available in the 'Broadband Amplifier Applications' booklet.

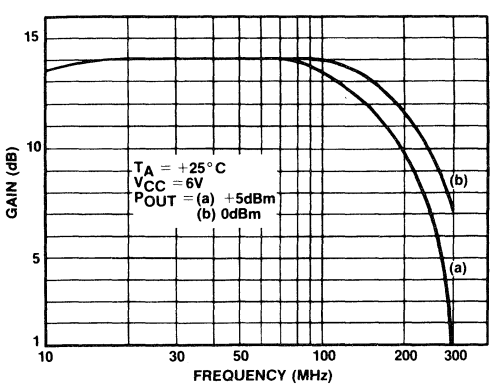


Fig.4 Frequency response, small signal gain is of a typical device

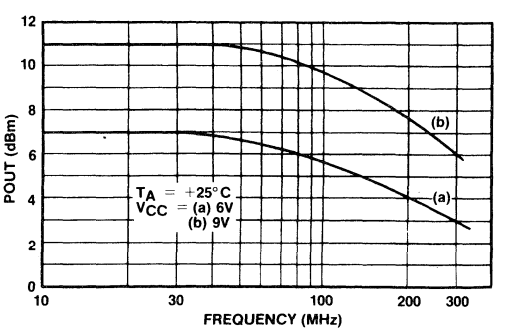


Fig.5 Frequency response, output capability (loci of maximum output power with frequency, for 1dB gain compression (typical)

TYPICAL APPLICATIONS

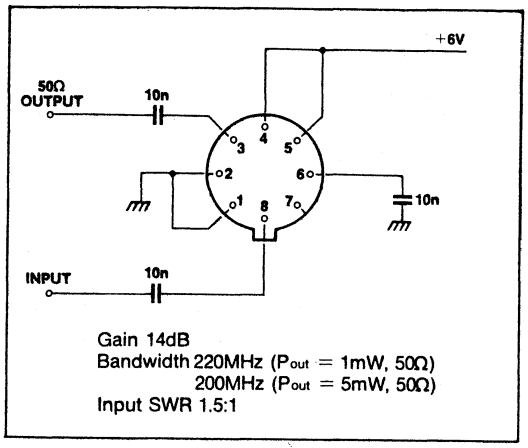


Fig.6 50Ω line driver. The response of this configuration is shown in Fig.4.

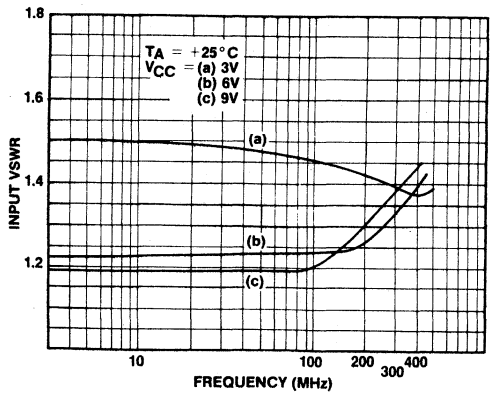


Fig.7 Input standing wave ratio plot of circuit shown in Fig.6 (typical)

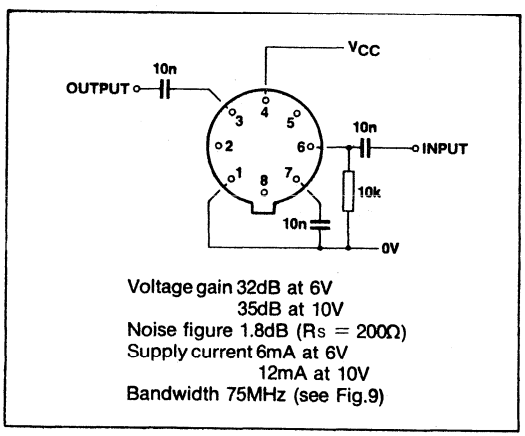


Fig.8 Low noise preamplifier

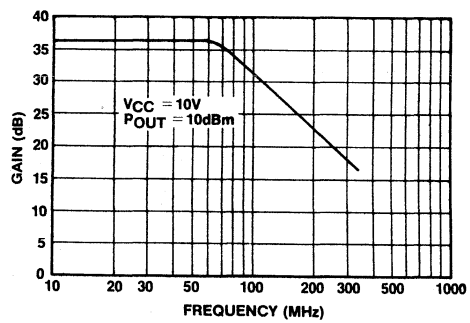


Fig.9 Frequency response of circuit shown in Fig.8 (typical)

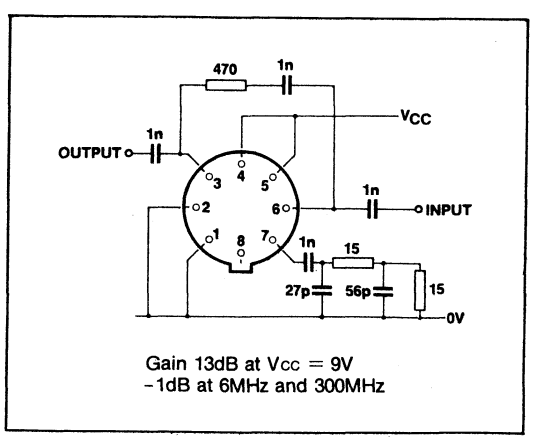


Fig.10 Wide bandwidth amplifier

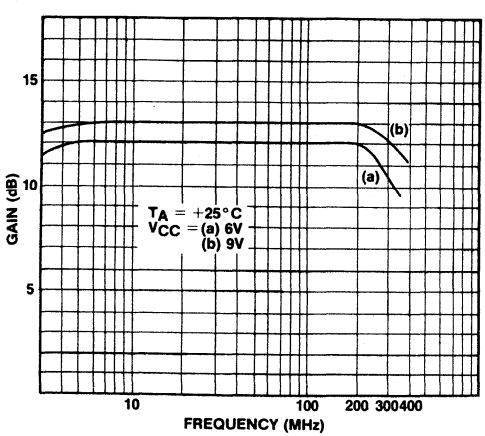


Fig.11 Frequency response of circuit shown in Fig.10 (typical)

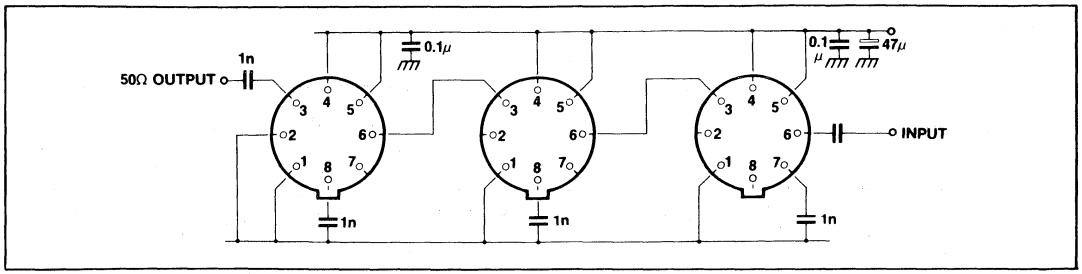


Fig.12 Three-stage directly-coupled high gain low noise amplifier

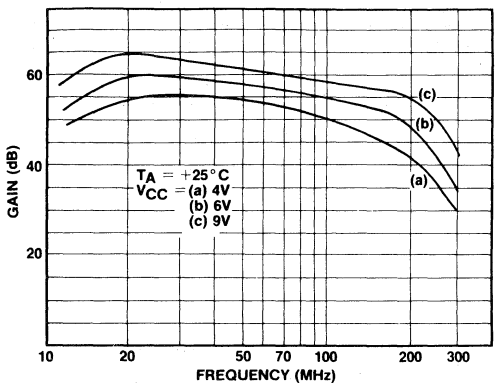


Fig.13 Frequency response of circuit shown in Fig.12 (typical)

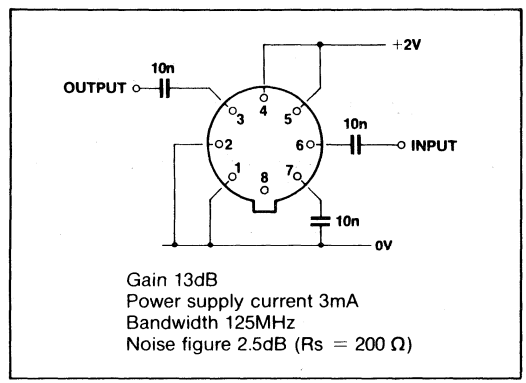


Fig.14 Low power consumption amplifier

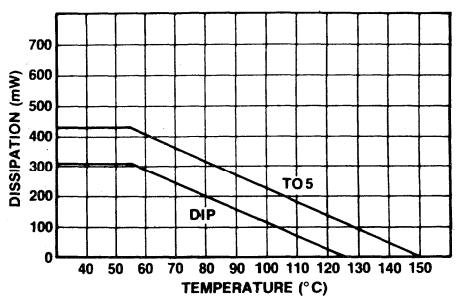


Fig.15 Ambient operating temperature v. degrees centigrade (typical)

DS 3298 -1

SL562

LOW NOISE PROGRAMMABLE OPERATIONAL AMPLIFIER

The SL562 is an advanced bipolar integrated circuit containing a single programmable operational amplifier. The amplifier can be programmed by current into a bias pin which determines the main characteristics of the amplifier's supply current, frequency response and slew rate. With a suitable choice of bias current the SL562 can be used where low power and low noise characteristics are a necessity.

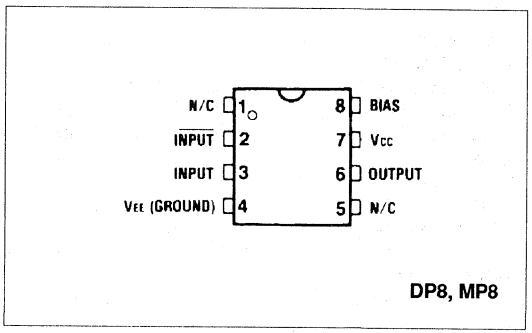


Fig. 1 Pin connections - top view

FEATURES

- Low Noise Guaranteed (25nV/√Hz at 1 kHz)
- Low Supply Current (40uA)
- Bias Conditions Adjustable to Optimise Performance
- Built In Short Circuit Protection
- Available In Small Outline

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers
- Frequency Synthesisers
- Hand Held Radio Applications

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±10V
- Supply Current ±40μA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB
- Operating Temperature Range -40°C to +85°C

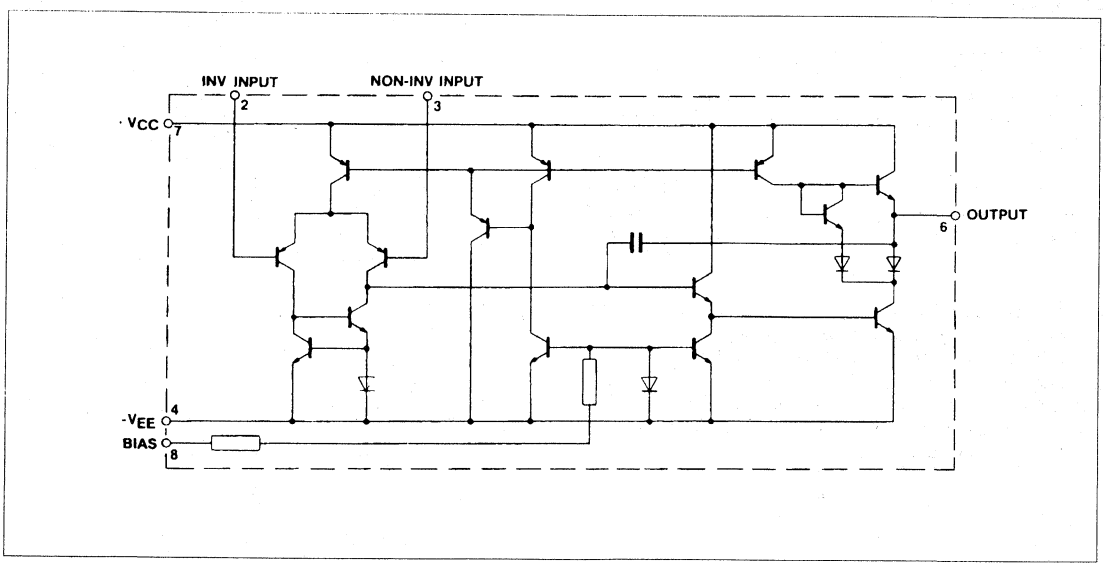


Fig. 2 Circuit diagram.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Operating mode A : Supply volts ±10V Bias set current 75μA
Operating mode B : Supply volts ±3.5V Bias set current 15μA
Operating mode C : Supply volts ±1.5V Bias set current 1μA

Characteristics	Operating mode									Units	Conditions
	A			B			C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage		1	5		1	5		1	5	mV	R_S = 10kΩ
Input offset current		20	190			150			49	nA	
Input bias current		250	800			350			95	nA	
Input resistance	0.1	0.6		0.2	0.5		0.3	2		MΩ	
Supply current	1000	1600	2200	50	200	1000	20	40	60	μA	
Large signal voltage gain	74	95		74	90		74	90		dB	R_L = 4kΩ(A) R_L = 100kΩ(B) R_L = 100kΩ(C)
Input voltage range	10	10.5		10	10.5		0.2	0.4		±V	R_S = 10kΩ
Common mode rejection ratio	70	110		70	85		70	82		dB	
Output voltage swing	8			1.5			0.7	0.8		±V	R_L = 4kΩ(A) R_L = 100kΩ(B) R_L = 100kΩ(C)
Supply voltage rejection ratio	74			85			85			dB	R_S = 10kΩ
Short circuit current	12		40				1	2.2		mA	T_{amb} = 0°C to +70°C
Gain bandwidth product		3.5			1			50		kHz MHz	Gain = 20dB
Slew rate		1.5			0.5			0.02		V/μs	Gain = 20dB
Input noise voltage		10	25		25	40		50	85	nV√Hz	f_o = 1kHz
Input noise current		1.6			1.6			1.0		pA√Hz	f = 1kHz

OPERATING NOTES

Bias set current

The amplifier is programmed by the ISET current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	ISET x 50kHz
Power supply current (each supply)	IsETx25,uA
Slewrate	ISETX0.02V/I1S (ISET inμA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 1 0,uA.

SincethevoltageontheBIASpinisapproximatelyO.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET}current is determined by:

$$I_{SET} = \frac{V_S - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken ower than 1V above the negative power supply.

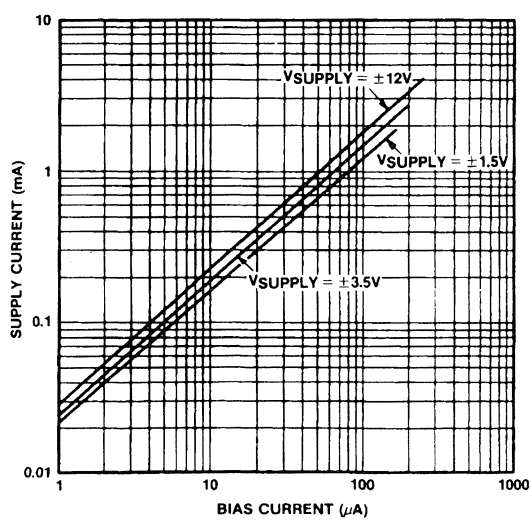


Fig. 3 Supply current v. bias set current

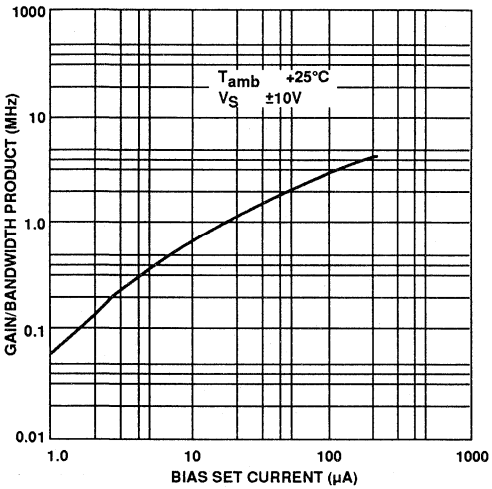


Fig. 4 Gain bandwidth product v. I_{SET}

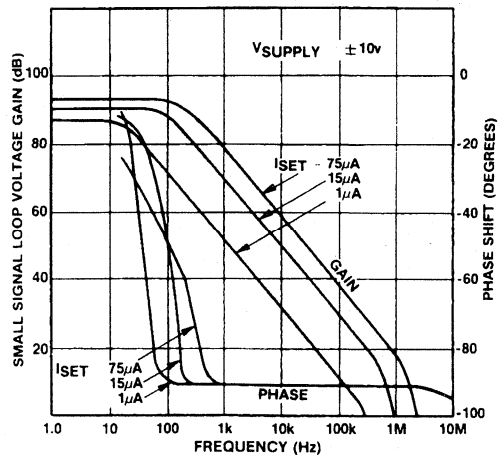


Fig. 5 Typical frequency response

APPLICATION EXAMPLE

The SL562 is especially suitable for use in loop filters for frequency synthesisers, the low noise and low power characteristics of the SL562 making it ideally suited for use with the GPS low power frequency synthesiser circuits (NJ8820, SP87XX). All three integrated circuits are available in surface mounting packages, thus making a compact hybrid.

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA
Storage	-55°C to +125°C
Power dissipation	800mW at 25°C
	Derate at 7mW/°C above 25°C
Operating temperature range	-40°C to +85°C

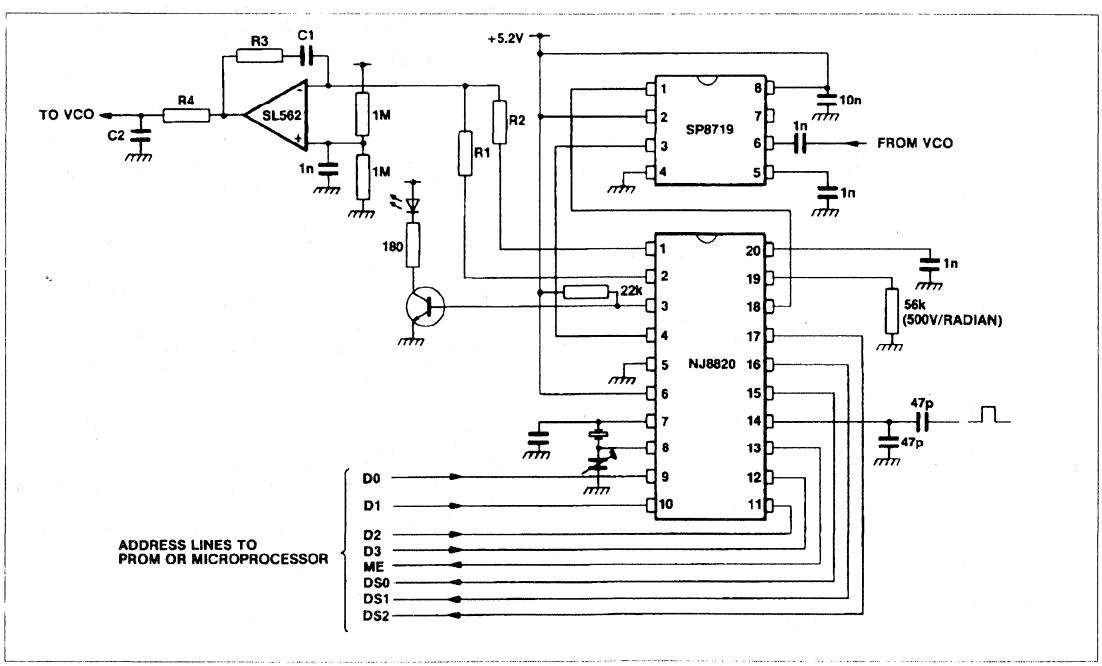


Fig. 6 Application example

DS 3299- 1

SL1610

RF/IF AMPLIFIER

The SL1610C RF voltage amplifier with AGC facilities. The voltage gain is 10 and the upper frequency response is 120MHz.

FEATURES

- Wide AGC Range: 50dB
- Easy Interfacing
- Integral Power Supply RF Decoupling

APPLICATIONS

- RF Amplifiers
- IF Amplifiers

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Voltage Gain: 17dB to 24dB

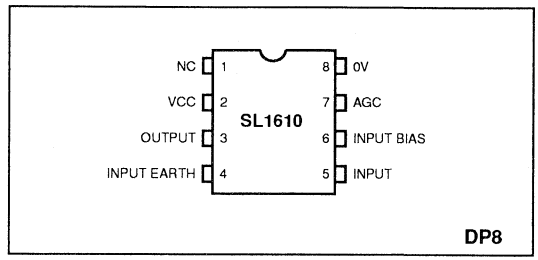


Fig.1 Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: -55°C to \+\125°C

ORDERING INFORMATION

SL1610C DP

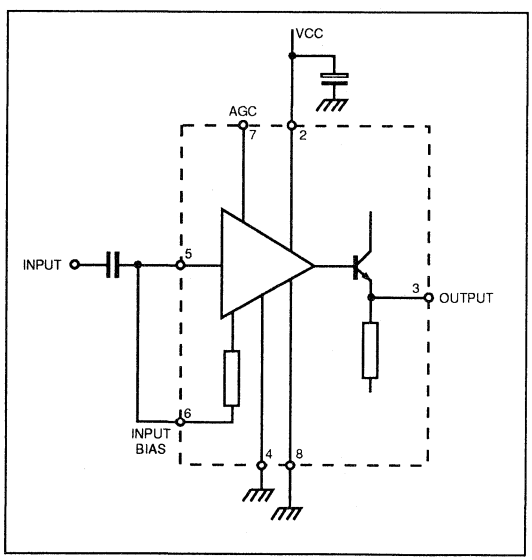


Fig.2 Block diagram

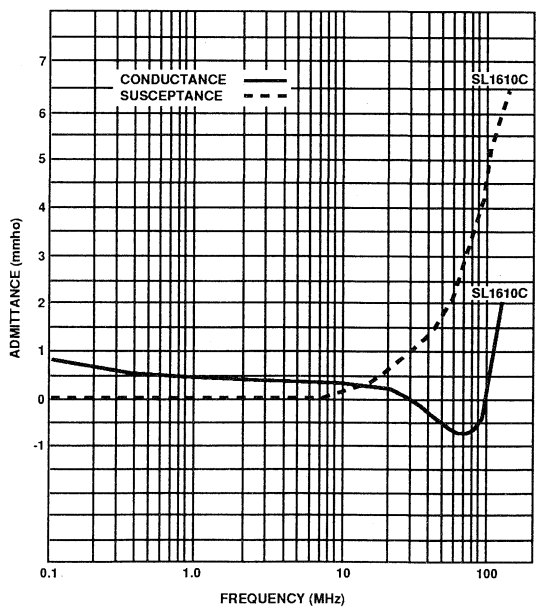


Fig.3 Input admittance with o/c output (G_{11})

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage VCC: 6V
Ambient temperature: -30°C to +85°C
Test frequency: SL1610C 30MHz

Characteristics	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL1610C		15	24	mA	
Voltage gain	SL1610C	17	20	24	dB	Rs = 50Ω
Cut-off frequency (-3dB)	SL1610C		120		MHz	
Max. output signal (max. AGC)			1.0		v rms	RL = 150Ω (SL1610C/1611C)) RL = 1.2kΩ (SL1612C)
Max.input signal (max. AGC)			250		mV rms	
AGC range	SL1610C	40	50		dB	
AGC current			0.15	0.6	mA	Current into pin 7 at 1.5V

APPLICATION NOTES

Input circuit

The SL1610C is normally used with pins 5 and 6 connected together and with the input connected via a capacitor as shown in Fig.2.

The input impedance is negative between 30MHz and 100MHz and is shown in Fig.3. the source is inductive is should be shunted by a 1kΩ resistor to prevent oscillation.

An alternative circuit with improved noise figure is shown in Fig.4.

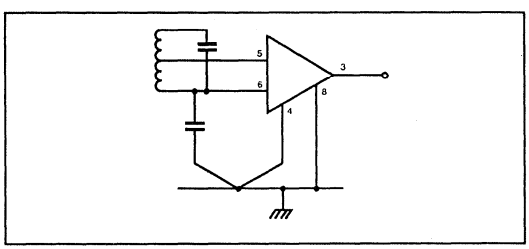


Fig.4 Alternative input circuit

Output circuit

The output stage is an emitter follower and has a negative output impedance at certain frequencies as shown in Fig.5.

To prevent oscillation when the load is capacitive a 47Ω resistor should be conncted in series with the output.

AGC

When pin 7 is open circuit or connected to a voltage less than 2V the voltage gain is normal. As the AGC voltage is increased there is a reduction in gain as shown in Fig.6. This reduction varies with temperature.

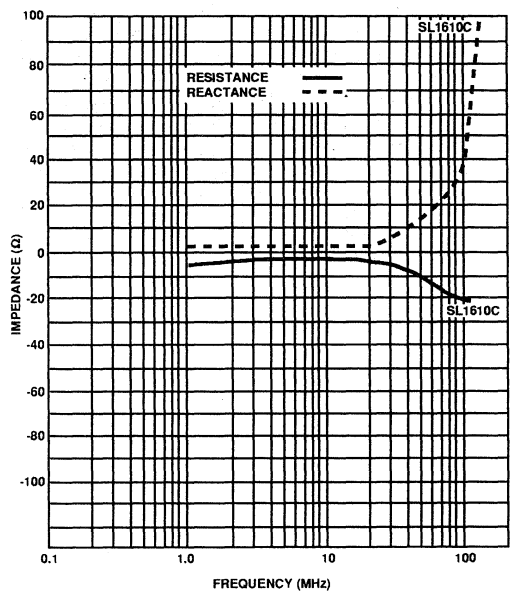


Fig.5 Typical output impedance with s/c input (G22)

Typical applications

The circuit of Fig.7 is a general purpose RF preamplifier. The voltage gain (from pin 5 to pin 3) is shown in Fig.8.

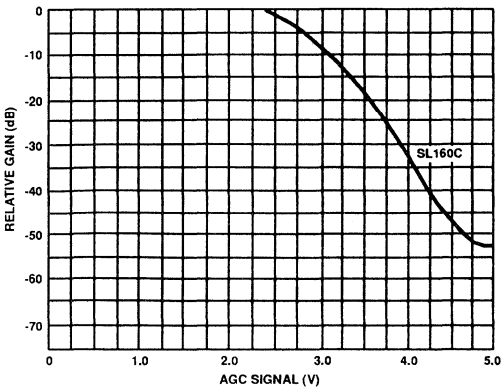


Fig.6 AGC characteristics (typical)

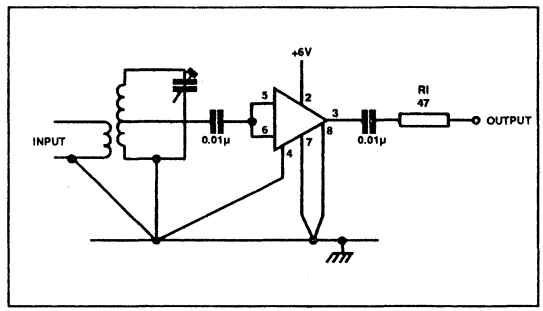


Fig.7 RF preamplifier

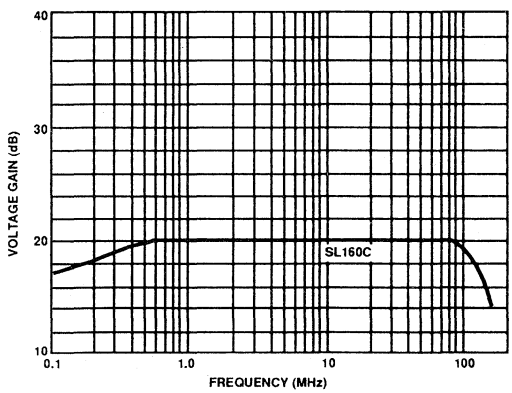


Fig.8 Typical voltage gain (RS = 50Ω)

DS 3305 -1

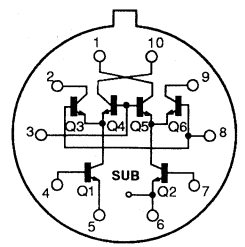
SL2363C & SL2364C

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

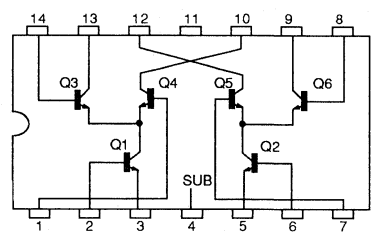
The SL2363C and SL2364C are arrays of transistors internally connected to form a dual long-tailed pair with tail transistors. They are monolithic integrated circuits manufactured on a very high speed bipolar process which has a minimum useable f_T of 2.5GHz, (typically 5GHz).

The SL2363 is in a 10 lead T05 encapsulation.

The SL2364 is in a 14 lead DIL plastic encapsulation and a high performance Dilmon encapsulation.



SL2363C **CM10**



DC14
DP14
MP14

SL2364C

Fig. 1 Pin connections (top view)

FEATURES

- Complete Dual Long-Tailed Pair in One Package
- Very High f_T - Typically 5 GHz
- Very Good MAtching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ±2°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10µA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5.0		V	I_E = 10µA
BV_{CIO}	16	40		V	I_C = 10µA
h_{FE}	50	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} (See note 1)		2	5	mV	I_C Tail) = 8mA, V_{CE} = 2V
$\Delta V_{BE} / T_{AMB}$		-1.7		mV/°C	I_C Tail) = 8mA, V_{CE} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0
C_{CI}		1.0	1.5	pF	V_{CI} = 0

NOTE 1. ΔV_{BE} applies to $| V_{BEQ3} - V_{BEQ4} |$ and $| V_{BEQ5} - V_{BEQ6} |$

TYPICAL CHARACTERISTICS

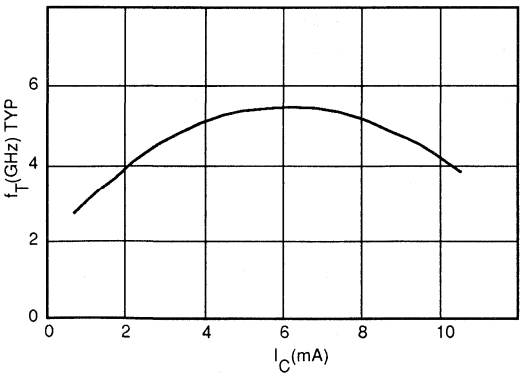


Fig. 2 Collector current

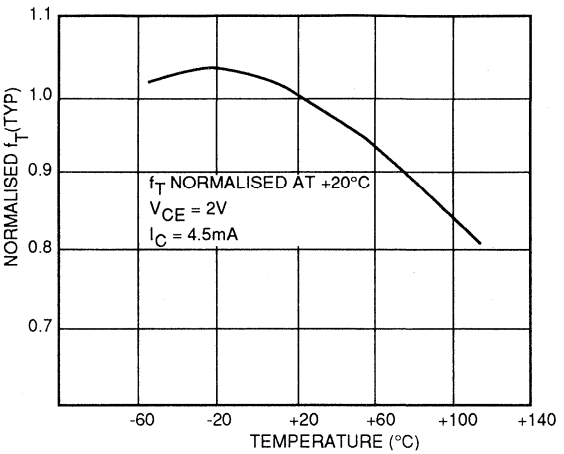


Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature -55°C to + 150°C
Maximum junction temperature + 150°C
Package thermal resistance (°C/W):
Chip to case 65 (CM10)
Chip to ambient 225 (CM10) 175 (DP14)
VCBO = 10V, VEBO = 2 5V VCEO = 6V. VCIO = 15V IC (any one transistor) = 20mA

The substrate should be connected to the most negative point of the circuit to maintain electrical isolation between the transistors.

DS 3306 -1

SL2365

VERY HIGH PERFORMANCE TRANSISTOR ARRAY

The SL2365 is an array of transistors internally connected to form a dual long-tail pair with current mirrors whose bases and collectors are connected internally. The ICs are manufactured on a very high speed bipolar process which has a minimum usable fT of 2.5GHz (typically 5GHz). The current mirror enables a well defined gain at low current levels to be achieved.

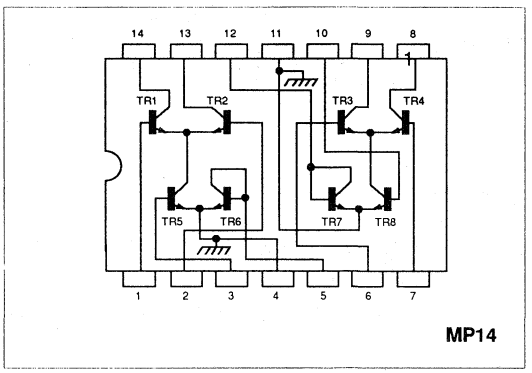


Fig. 1 Pin connections (top view)

FEATURES

- Complete Dual Long Tailed Pair in One Package
- Very High fT - Typically 5GHz
- Well Defined Gain at Low Current Levels
- Available in Small Outline Package

CAUTION

Pins 4 and 11 should be equal and at the most negative voltage on the array.

ELECTRICAL CHARACTERISTICS

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10µA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5		V	I_E = 10µA
BV_{CIO}	16	40		V	I_C = 10µA
H_{fe}	50	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C Tail) = 8mA, V_{CE} = 2V
ΔV_{BE}		2	5	mV	I_C Tail) = 8mA, V_{CE} = 2V
$\Delta V_{BE} / T_{AMB}$		-7		mV/°C	I_C Tail) = 8mA, V_{CE} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0
C_{CI}		1.0	1.5	pF	V_{CI} = 0

DS 2451 -2

SL2366

HIGH PERFORMANCE TRANSISTOR ARRAY

The SL2366 is an array of transistors internally connected to form a dual long-tail pair. The ICs are manufactured on a high speed bipolar process, which has a minimum usable f_T of 2.5GHz (typically 5GHz).

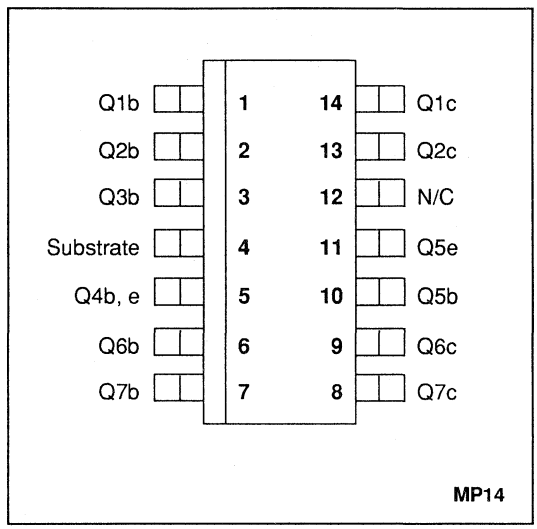


Figure 1 : Pin connections - top view

FEATURES

- Complete Dual Long Tailed Pair in One Package
- Very High f_T - Typically 5GHz
- Well Defined Gain at Low Current Levels
- Available in Small Outline Package
- 3:1 current mirror formed by Q3, Q4

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation	200mW
Storage temperature	-55°C to +150°C
Maximum junction temperature	+150°C

Package thermal resistance (°C/W):
Chip to ambient 200

V_{CBO} = 10V, V_{EBO} = 2.4V, V_{CEO} = 6V, V_{CIO} = 15V, IC (any one transistion) = 20mA

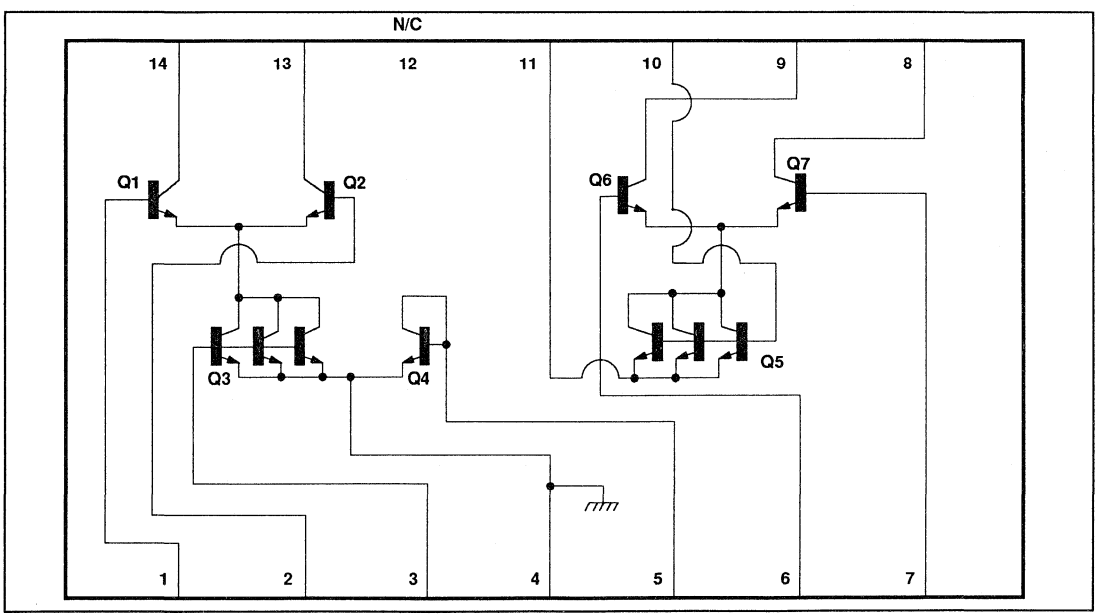


Figure 2 : SL2366 Circuit Diagram

ELECTRICAL CHARACTERISTICS Q1 - Q7

T_{amb} = 22°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BVcbo	10	20		V	I_C = 10µA
LVceo	6	9		V	I_C = 5mA
BVcbo	2.5	5		V	I_E = 10µA
BVcio	16	40		V	I_C = 10µA
Hfe	50	80			I_C = 8mA, V_{ce} = 2V
fT	2.5	5		GHz	I_C(tail) = 8mA, V_{ce} = 2V
$\Delta V_{be}/T_{amb}$		2.0	5.0	mV	I_C(tail) = 8mA, V_{ce} = 2V
$\Delta V_{be}/T_{amb}$		-7.0		mV/°C	I_C(tail) = 8mA, V_{ce} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0V (note 1)
C_{CI}		1.0	1.5	pF	V_{CI} = 0V (note 1)

Note 1 Parameters guaranteed by design, not production
Note2 Pin 4 must be connected to the most negative part of the circuit

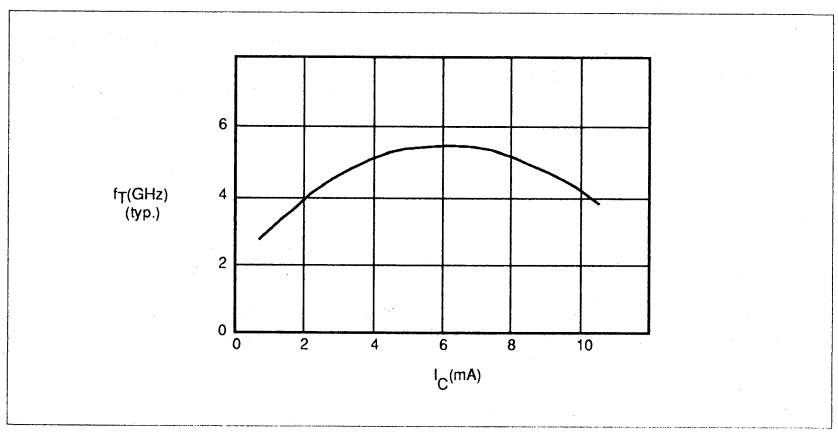


Figure 3 : Collector Current

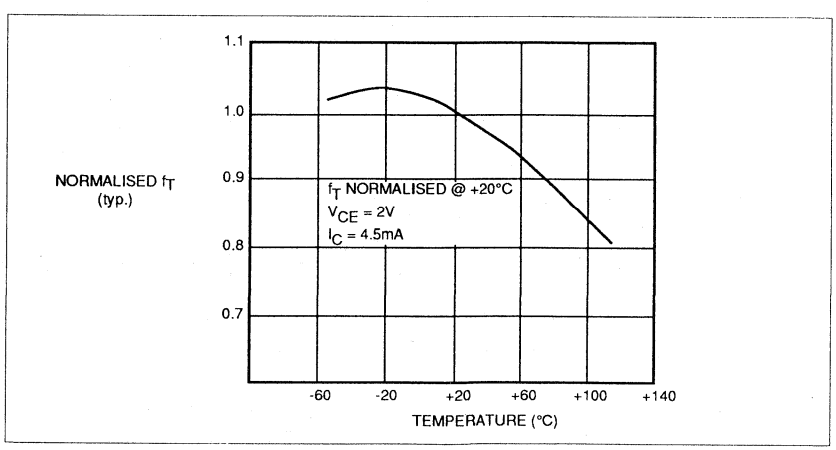


Figure 4 : Chip Temperature

2159 2.4

SL6140

400MHz WIDEBAND AGC AMPLIFIER

(Supersedes Edition in May 1991 Professional Products IC Handbook)

The SL6140 is an integrated broadband AGC amplifier, designed on an advanced 3-micron all implanted bipolar process. The amplifier provides over 15dB of linear gain into 50Ω at 400MHz.

Accurate gain control is also provided with over 70dB of dynamic range.

The SL6140 provides over 45dB of voltage gain with an R_L of 1kΩ.

FEATURES

- 400MHz Bandwidth (R_L = 50Ω)
- High Voltage Gain 45dB (R_L = 1kΩ)
- 70dB Gain Control Range
- High Output Level at Low Gain
- Accurate Gain Control
- Full Military Temperature Range (CM only)
- MC1590 Replacement with Improved Performance in most applications

APPLICATIONS

- RF/IF Amplifier
- High Gain Mixers
- Video Amplifiers

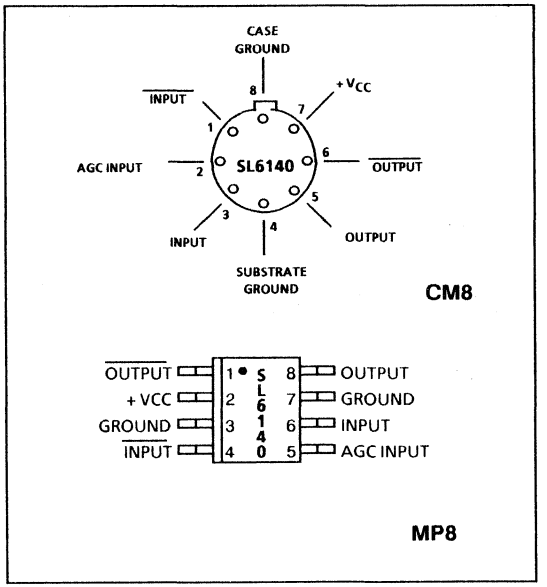


Fig.1 Pin connections - top view

ORDERING INFORMATION

SL6140 NA MP	Industrial temperature range, miniature plastic package.
SL6140 A CM	Military temperature range, metal can package
SL6140 AC	MIL-STD-883 " CLASS B" compliant, metal can package.

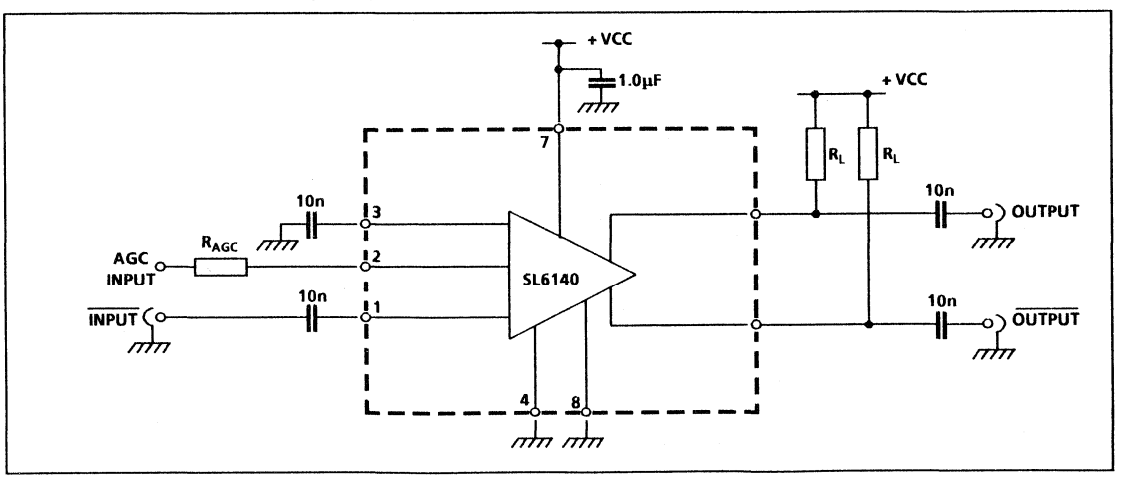


Fig.2 Typical application (CM pinout)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 25°C, V_{CC} = 12V ±5%, V_{IN} = 1mV_{RMS}, Frequency = 6MHz, Load (R_L) = 1KOHms, R_{AGC} = 22KOHm

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	5,6,7		19	23	mA	No input signal
Output stage current	5,6 (sum)	5	7	9	mA	No input signal
Output current matching (magnitude of difference of output currents)	5,6		1.0		mA	See note 2
AGC range	2	60	75		dB	See Fig. 4 & Note 1 (VAGC = 0V to 10V)
Voltage gain (single ended)	5,6	40	45		dB	R_L = 1kΩ See Fig. 5 & Note 1
			55		dB	Tuned input and Output
	5,6		15		dB	R_L = 50Ω
Bandwidth (-3dB)	5,6		25		MHz	RL = 1kΩ See Fig. 5 See note 2
			400			RL = 50Ω
Maximum output level (single ended)						
0dB AGC	5,6	2.5	3.5		V p-p	Note 1
-30dB AGC	5,6	2.5	3.5		V p-p	R_L = 1kΩ. Note 1
Noise figure	5,6		5		dB	Test CCT Fig. 13
Gain change with temp.	5,6		+4.5		dB	At -55°C W.R.T R/T See note 2
V_{AGC} = 9V	5,6		-3		dB	At +125°C W.R.T R/T See note 2
Gain change with temp.	5,6		+2		dB	At -55°C W.R.T R/T See note 2
V_{AGC} = 10V	5,6		-3		dB	At +125°C W.R.T R/T See note 2

Note: 1 Guaranteed but not tested for MP package

Note: 2 Guaranteed but not tested

DESCRIPTION

The SL6140 (Fig. 3) is a high gain amplifier with an AGC control capable of reducing the gain of the amplifier by over 70dB. The gain is adjustable by applying a voltage to the AGC input via an external resistor (R_{AGC}), the value of which adjusts the curve of gain reduction versus control voltage (see Fig. 4). As the output stage of the amplifier is an open collector the maximum voltage gain is determined by R_L. With load resistance of 1kΩ the single ended voltage gain is 45dB and with a load resistance of 50Ω the voltage gain is 15dB ($20\log_{10} V_{OUT}/V_{IN}$). Another parameter that depends on the load resistance is the bandwidth: 25MHz for R_L = 1kΩ, as compared with 400MHz for R_L = 50Ω. R_L is chosen to give either the required bandwidth or voltage gain for the circuit.

Figs. 7 through to 10 show the typical S parameters for the device. Figs 11 and 12 show the typical variation in 3rd order intercept performance with AGC.

In any application, the substrate (pin 4 in CM 8, pin 7 in MP 8) should be connected to the most negative point in the circuit, usually to the same point as pin 8 (pin 3 in MP 8).

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+18V
Input voltage (differential)	+5V
AGC supply	V_{CC}
Storage temperature	-55°C to +150°C
Operating temperature range	
SL6140 MP	-40°C to +85°C
SL6140 A CM	-55°C to +125°C at 200mW
Chip operating temperature	
SL6140 MP	+150°C
SL6140 (CM variants)	+175°C

THERMAL RESISTANCE

Chip-to-ambient	
SL6140 MP	163°c/w
SL6140 (CM variants)	225°C/W
Chip-to-case	
SL6140 MP	57°C/W
SL6140 (CM variants)	65°C/W

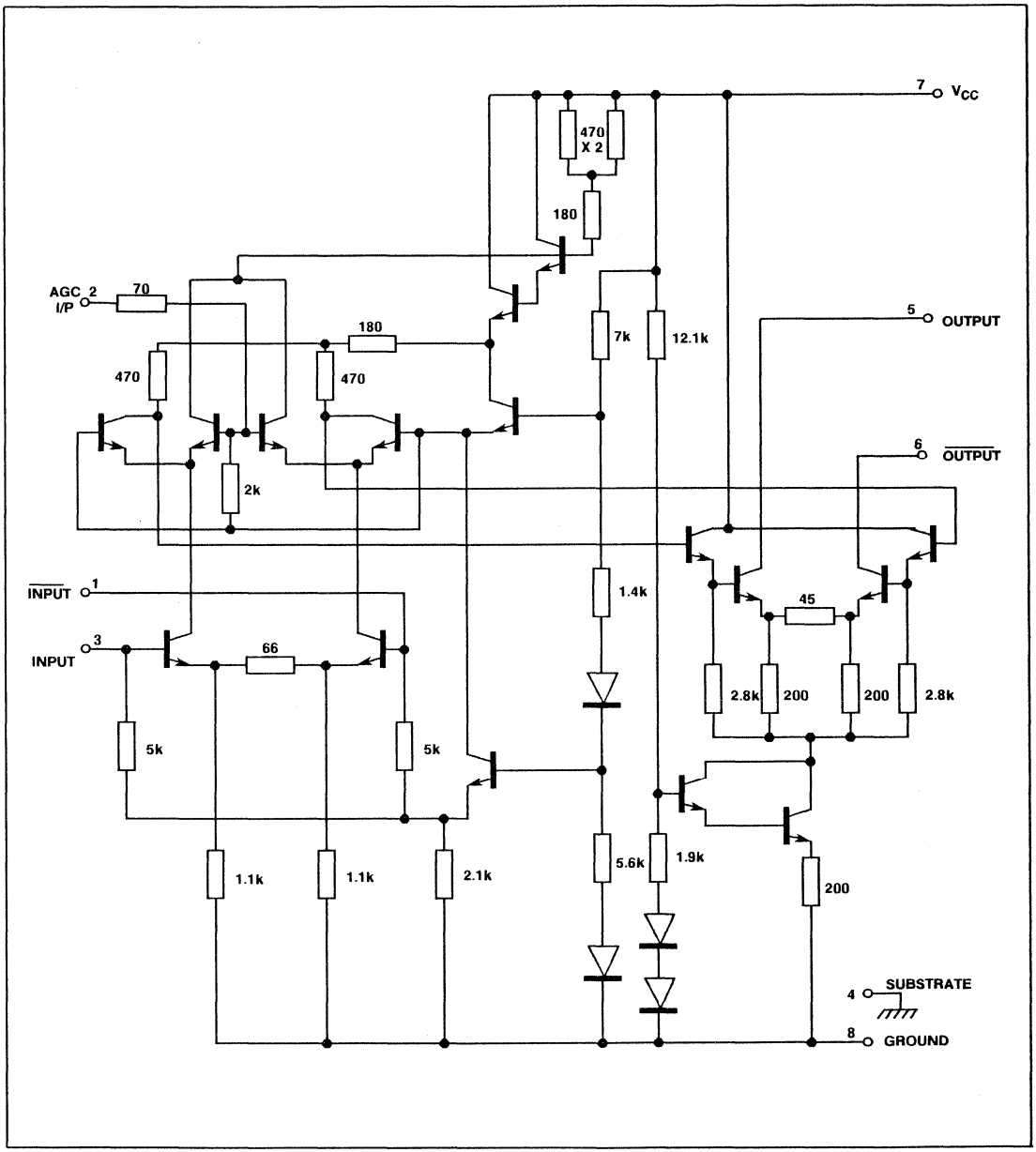


Fig. 3 Full circuit diagram of SL6140 (CM pinout)

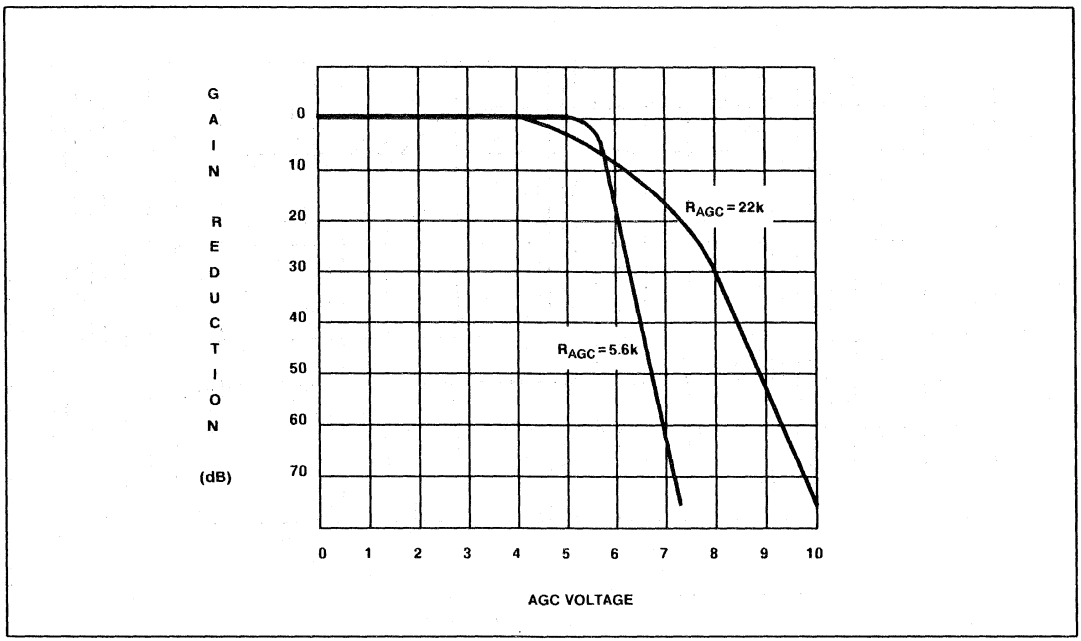


Fig. 4 Gain reduction v. AGC voltage

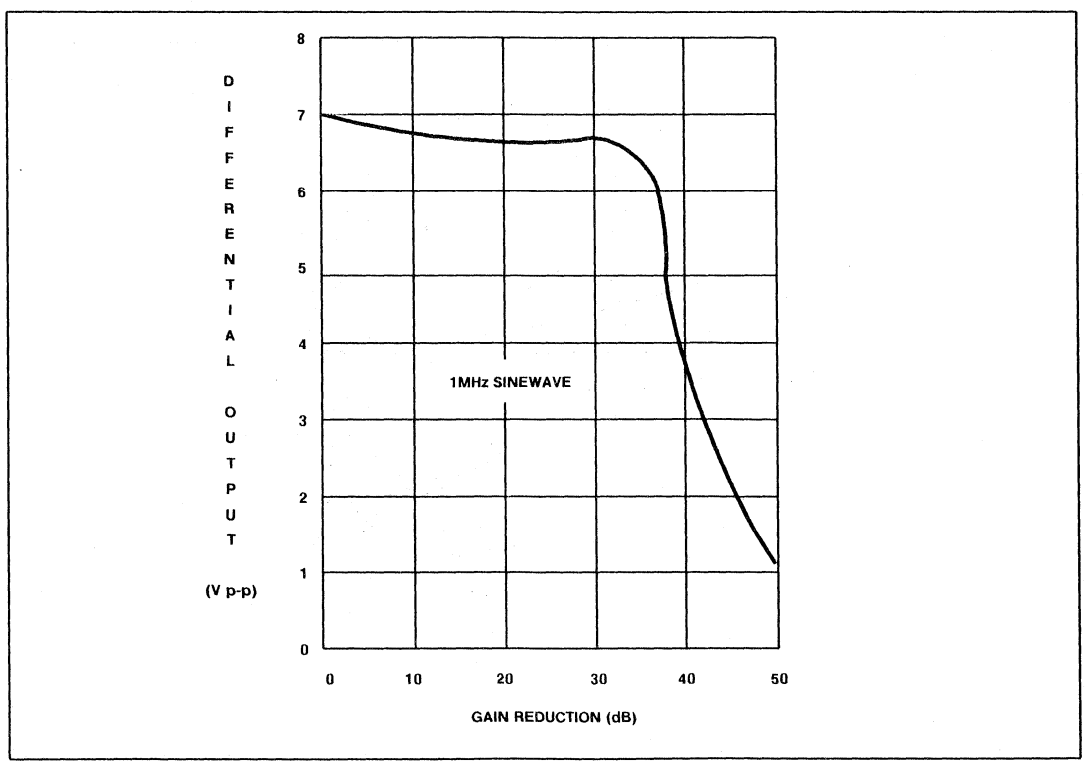


Fig. 5 Max differential O/P voltage v gain reduction

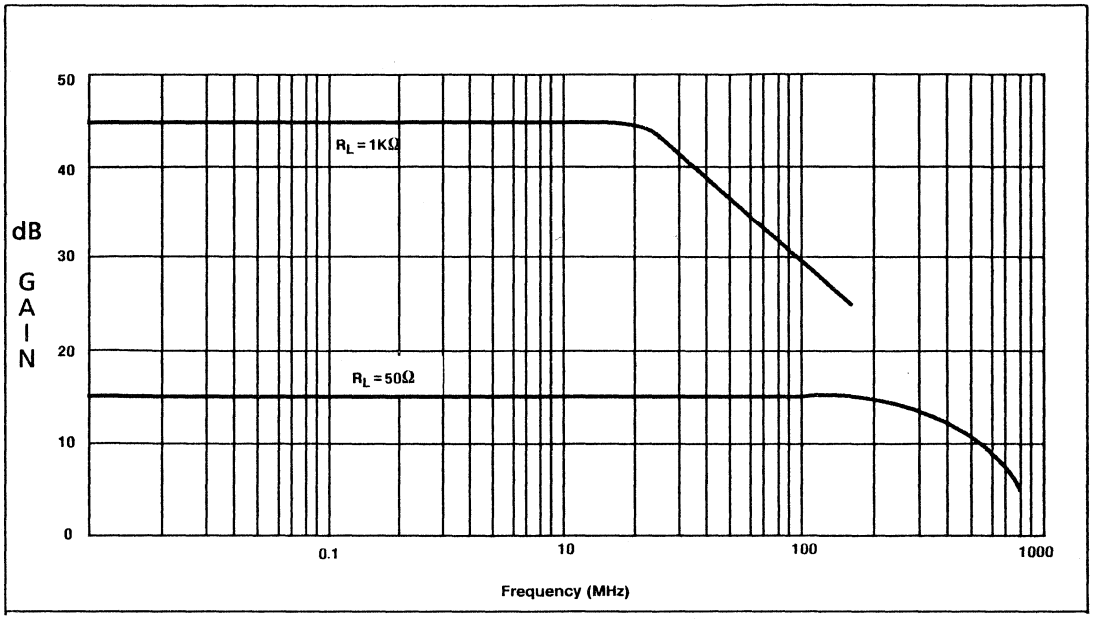


Fig. 6 Voltage Gain V. Frequency

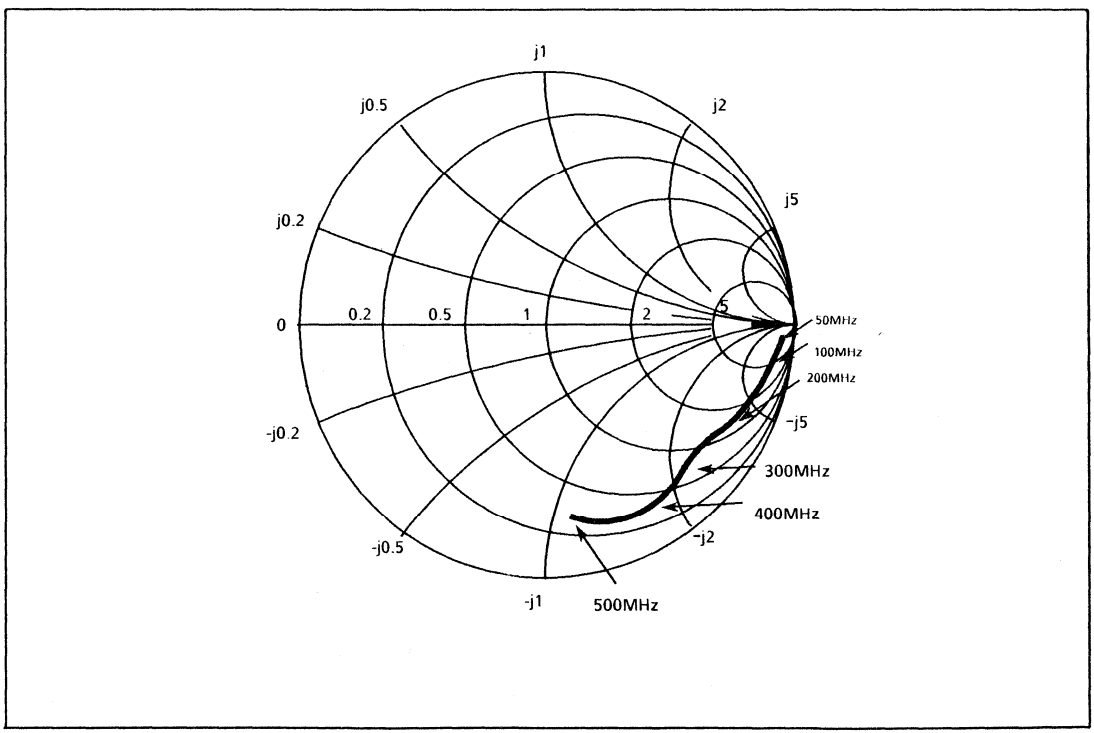


Fig. 7 Input impedance 50Ω system

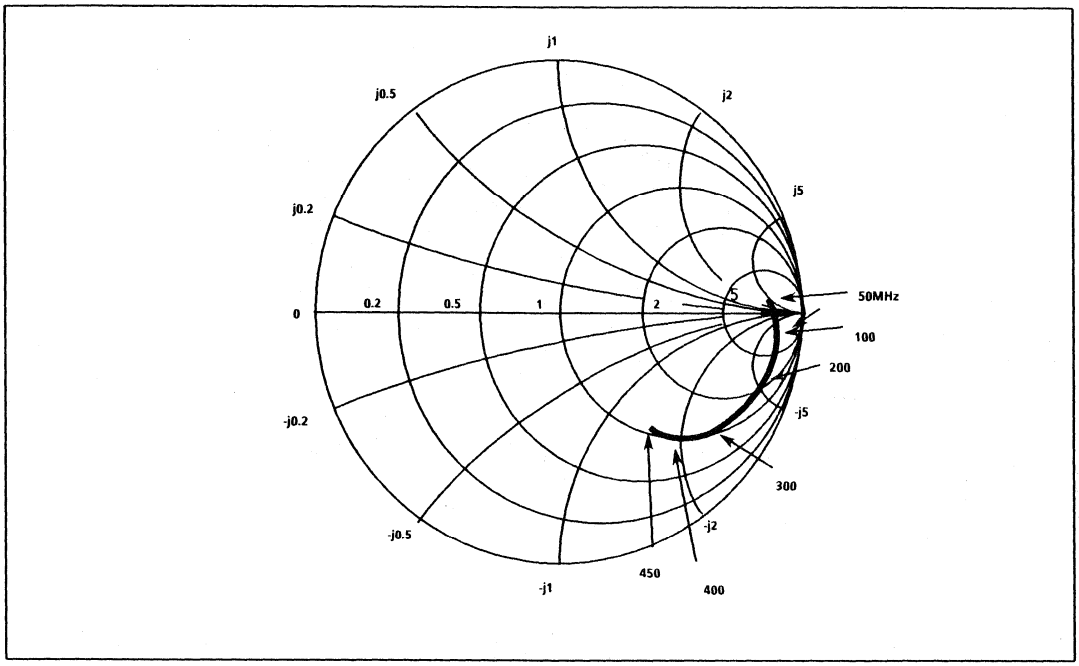


Fig. 8 Output impedance 50Ω system

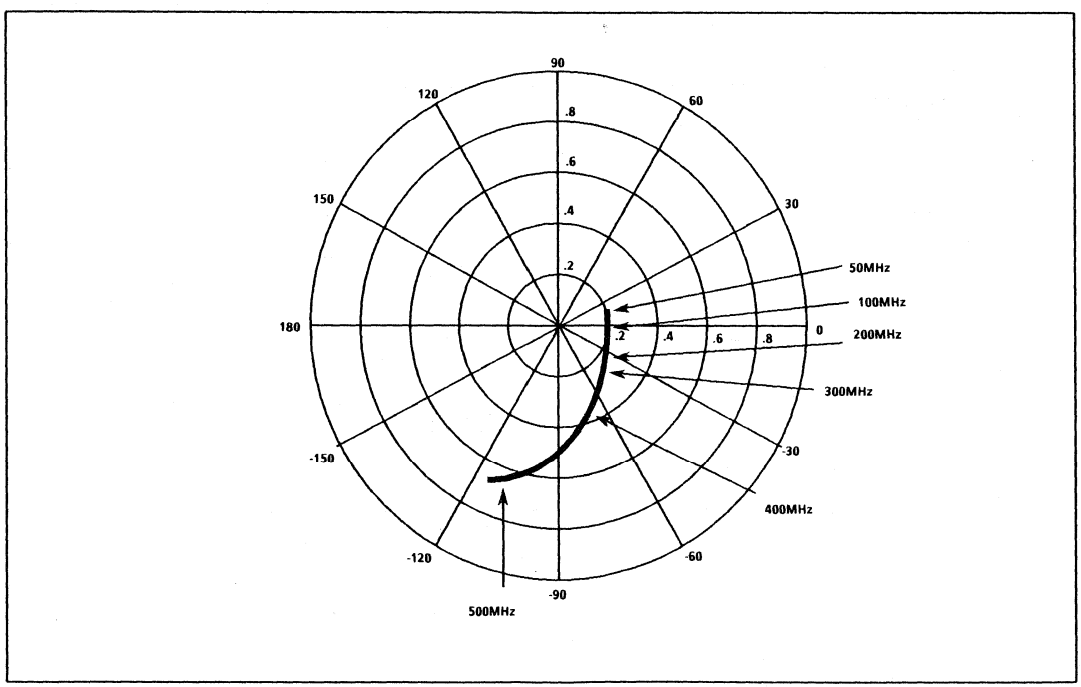


Fig. 9 Reverse transmission coefficient S_{12} SL6140

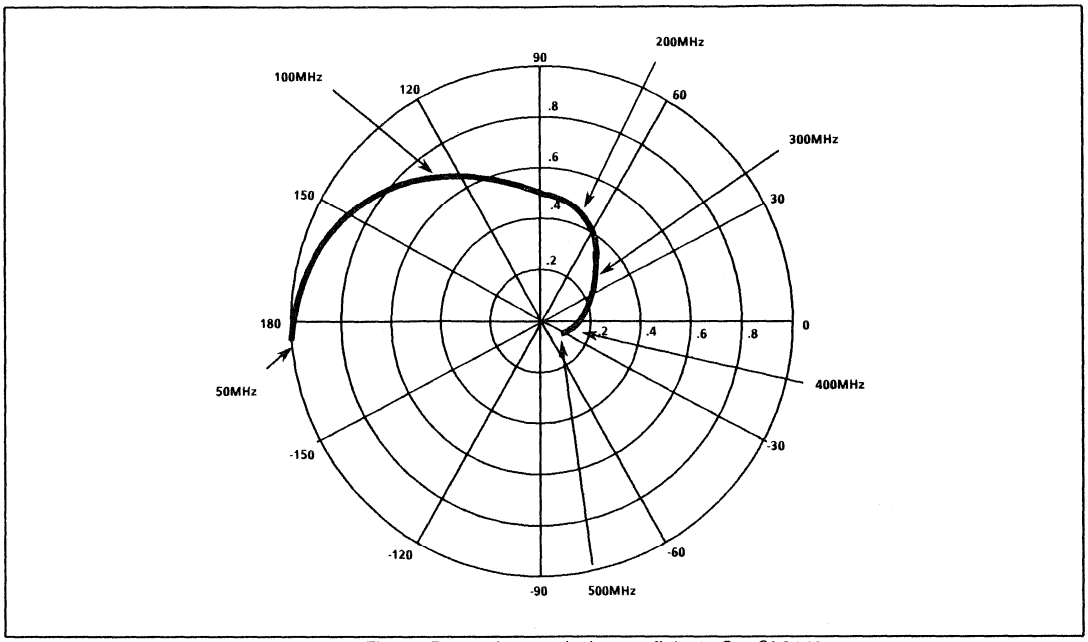


Fig.10 Forward transmission coeficients S_{21} SL6140

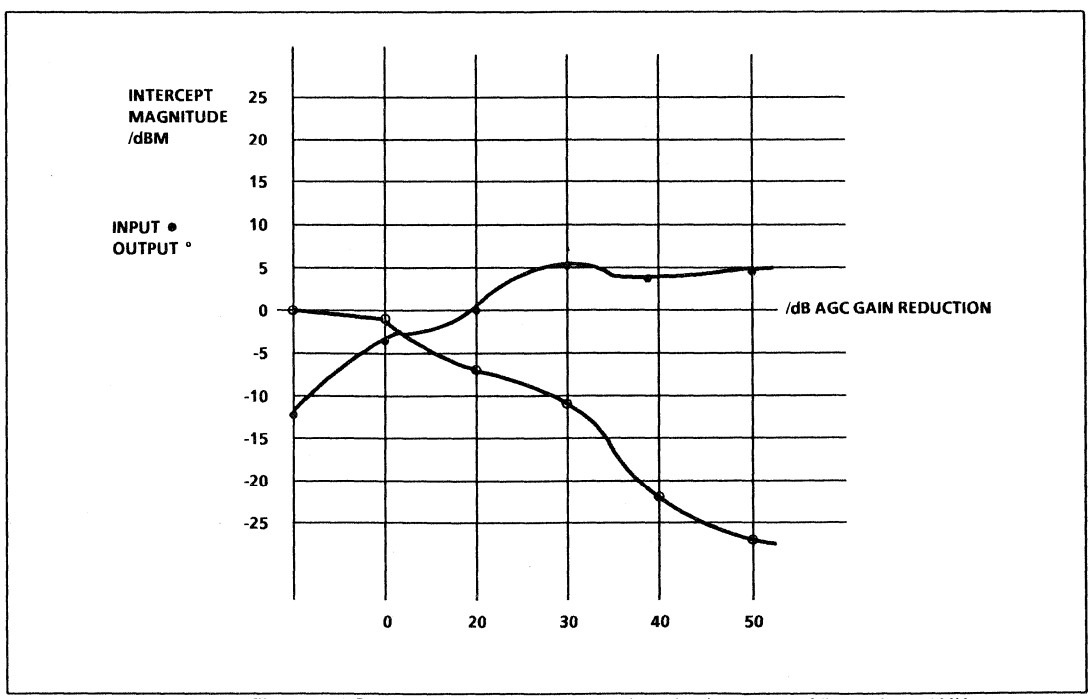


Fig.11 3rd Order intercept point against gain reduction at 250.0Mhz and 254.0MHz

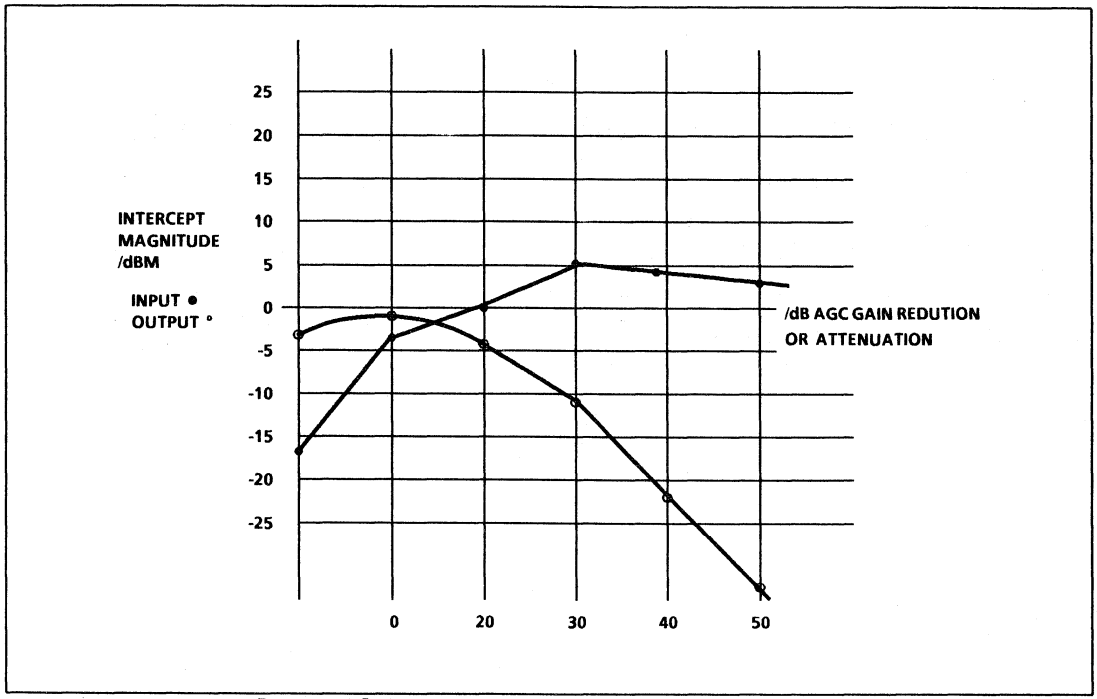


Fig.12 3rd Order intercept point against gain reduction at 100.0Mhz and 104.0MHz

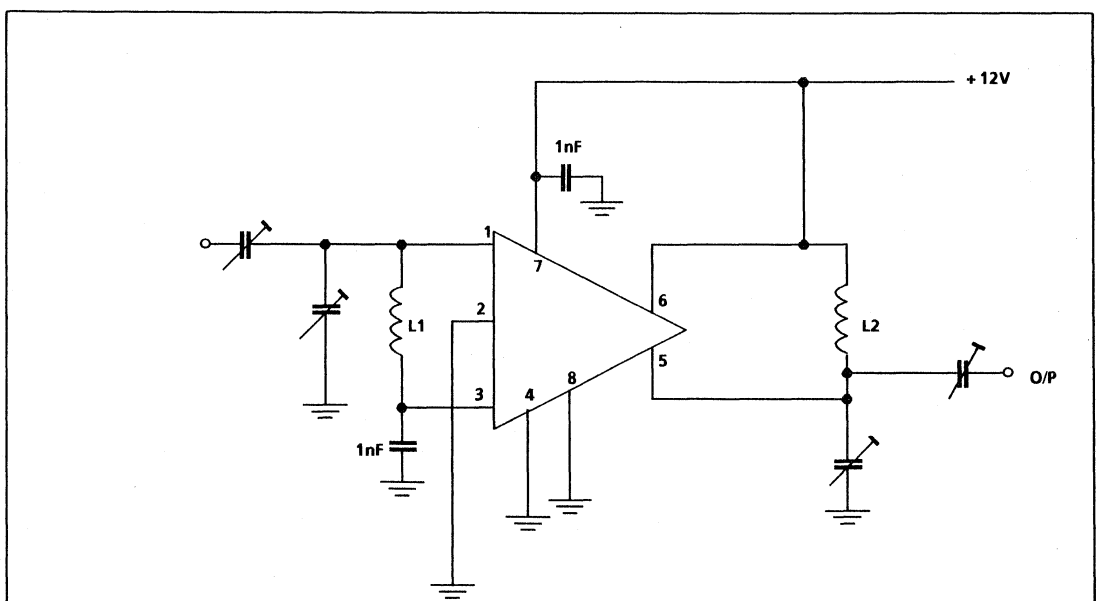


Fig.13 50MHz Noise figure test circuit CM package)

SL6270C

GAIN CONTROLLED MICROPHONE PREAMPLIFIER/VOGAD

The SL6270 is a silicon integrated circuit combining the functions of audio amplifier and voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low sensitivity microphone and to provide an essentially constant output signal for a 50dB range of input. The dynamic range, attack and decay times are controlled by external components.

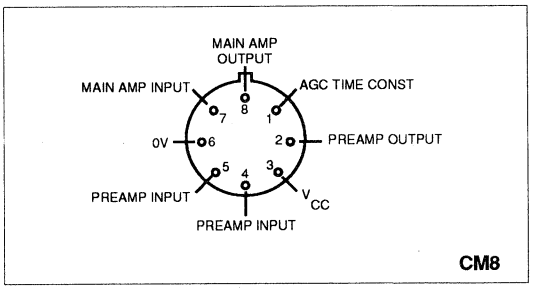


Fig. 1 Pin connections, SL6270 - CM (bottom view)

FEATURES

- Constant Output Signal
- Fast Attack
- Low Power Consumption
- Simple Circuitry

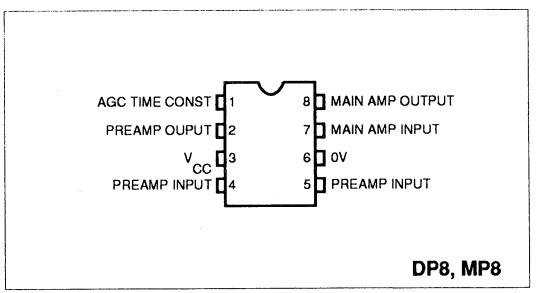


Fig. 2 Pin connections, SL6270 - DP (top view)

APPLICATIONS

- Audio AGC Systems
- Transmitter Overmodulation Protection
- Tape Recorders

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 10V
- Voltage Gain: 52dB

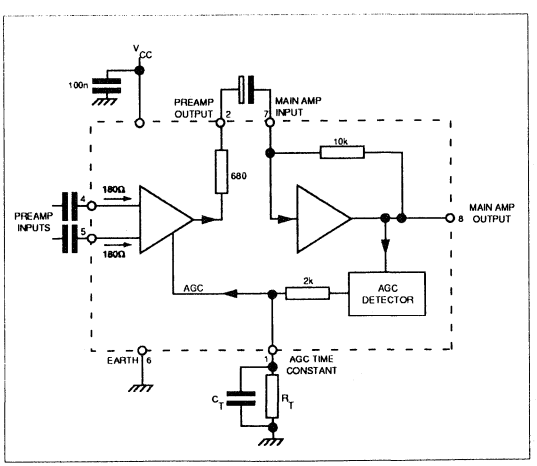


Fig. 3 SL6270 block diagram

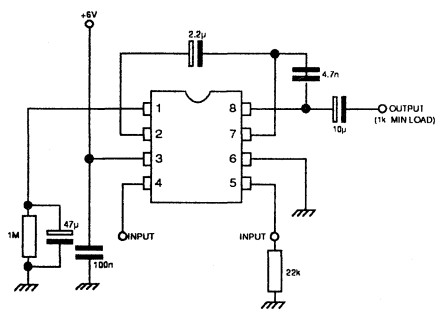
ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: -55°C to +125°C

ELECTRICAL CHARACTERISTICS

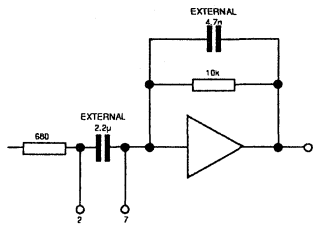
Test conditions (unless otherwise stated):
Supply voltage Vcc: 6V
Input signal frequency: 1kHz
Ambient temperature: -30°C to +85°C
Test circuit shown in Fig. 4

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5	10	mA	
Input impedance		150		Ω	Pin 4 or 5
Differential impedance		300		Ω	
Voltage gain	40	52		dB	72μV rms input pin 4
Output level	55	90	140	mV rms	4MV rms input pin 4
THD		2	5	%	90mV rms input pin 4
Equivalent noise input voltage		1		μV	300Ω source, 400Hz to 25kHz bandwidth



N.B. If input not AC coupled the resistance between pins 4 and 5 must be less than 10 ohms.

Fig. 4 SL6270 test and application circuit



Voltage gain = $\frac{10k\Omega}{680\Omega}$

Upper frequency response 10kΩ/4.7nk = 3kHz
Lower frequency response 680Ω/2.2μF = 300Hz

Fig. 5 SL6270 frequency response

APPLICATION NOTES

Voltage gain

The input to the SL6270 may be single ended or differential but must be capacitor coupled. In the single-ended mode the signal can be applied to either input, the remaining input being decoupled to ground. Input signals of less than a few hundred microvolts rms are amplified normally but as the input level is increased the AGC begins to take effect and the output is held almost constant at 90mV rms over an input range of 50dB.

The dynamic range and sensitivity can be reduced by reducing the main amplifier voltage gain. The connection of a lk resistor between pins 7 and 8 will reduce both by approximately 20dB. Values less than 680Ω are not advised.

Frequency response

The low frequency response of the SL6270 is determined by the input, output and coupling capacitors. Normally the coupling capacitor between pins 2 and 7 is chosen to give a -3dB point at 300Hz, corresponding to 2.2,μF, and the other capacitors are chosen to give a response to 100Hz or less.

The SL6270 has an open loop upper frequency response of a few MHz and a capacitor should be connected between pins 7 and 8 to give the required bandwidth.

Attack and delay times

Normally the SL6270 is required to respond quickly by holding the output level almost constant as the input is increased. This 'attack time', the time taken for the output to return to within 10% of the original level following a 20dB increase in input level, will be approximately 20ms with the circuit of Fig.4. It is determined by the value of the capacitor connected between pin 1 and ground and can be calculated approximately from the formula:

Attack time = 0.4ms/μF

The decay time is determined by the discharge rate of the capacitor and the recommended circuit gives a decay rate of 20dB/second. Other values of resistance between pin 1 and ground can be used to obtain different results.

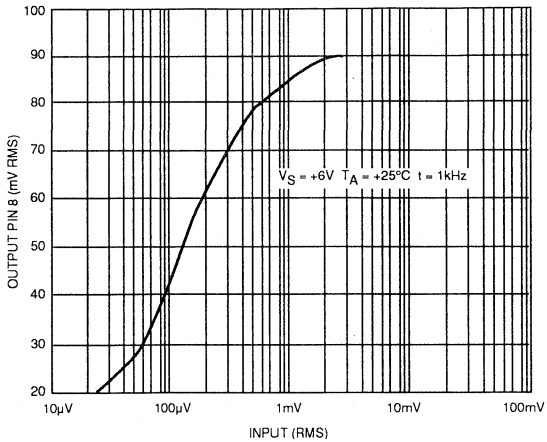


Fig. 6 Voltage gain (single ended input) (typical)

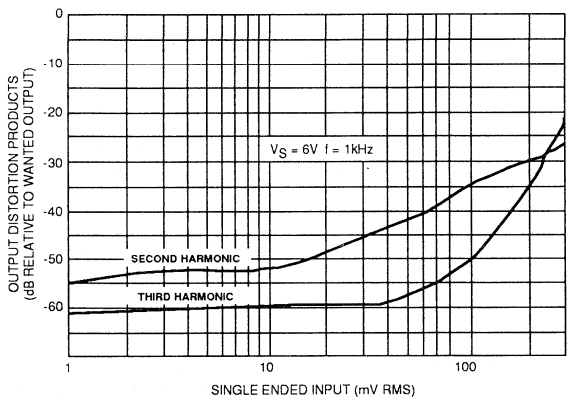


Fig. 7 Overload characteristics (typical)

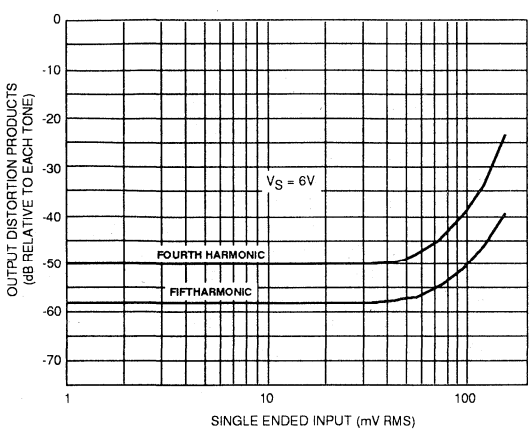


Fig. 8 Typical Intermodulation distortion (1.55 and 1.85kHz tones)

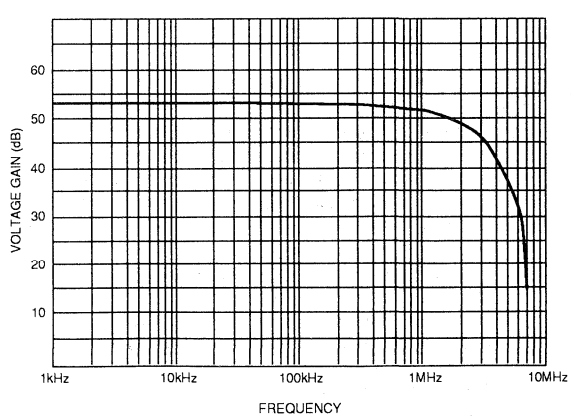


Fig. 9 Open loop frequency response (typical)

DS 3302 -1

SL6310C

500mW SWITCHABLE AUDIO AMPLIFIER/OP AMP

The SL6310C is a low power audio amplifier which can be switched off by applying a mute signal to the appropriate pin. Despite the low quiescent current consumption of 5mA (only 0.6mA when muted) a minimum output power of 400mW is available into an 8Ω load from a 9V supply.

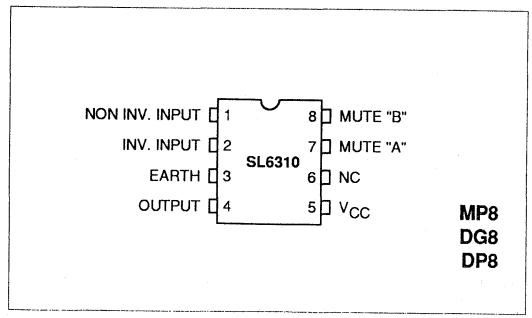


Fig. 1 Pin connections, SL6310 - (top view)

FEATURES

- Can be Muted with High or Low State inputs
- Operational Amplifier Configuration
- Works Over Wide Voltage Range

APPLICATIONS

- Audio Amplifier for Portable Receivers
- Power Op. Amp
- High Level Active Filter

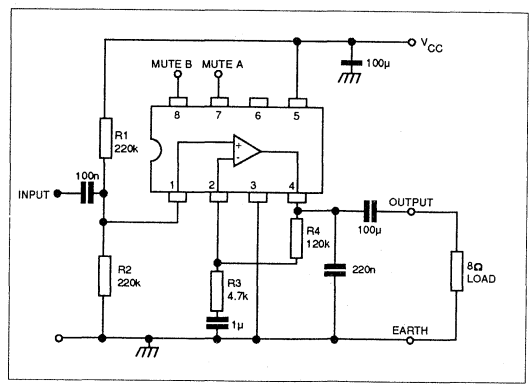


Fig. 2 SL6310 Test Circuit

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 13.6V
- Voltage Gain: 70dB
- Output into 8Ω on 9V Supply : 400mW (min.)

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 15V
Storage temperature: —55°C to + 125°C

SL6310C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage Vcc: 7V
Ambient temperature: -30°C to +85°C
Mute facility : Pins 7 and 8 open circuit frequency = 1kHz

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.0	7.5	mA	
Supply current mute (A)		0.55	1	mA	Pin 7 via 470k to earth
Supply current mute (B)		0.6	0.9	mA	Pin 8 = V_{CC}
Input offset voltage		2	20	mV	$R_S \leq 10k$
Input offset current		50	500	nA	
Input bias current (Note 1)		0.2	1	µA	
Voltage gain	40	70		dB	
Input voltage range		2.1		V	V_{CC} = 4.5V
		10.6		V	V_{CC} = 13V
CMRR	40	60		dB	$R_S \leq 10K$
Output power	400	500		mW	$R_L = 8\Omega$
THD		0.4	3	%	P_{OUT} = 400mW, Gain = 28dB

NOTE

1. The input bias current flows **out** of pins 1 and 2 due to PNP input stage

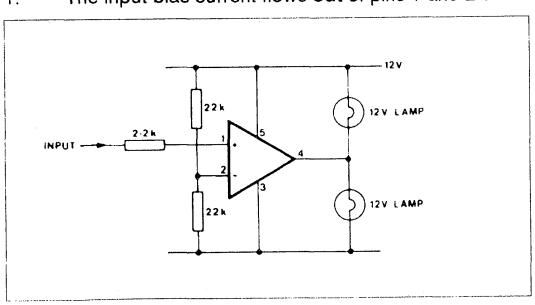


Fig. 3 SL6310 lamp driver

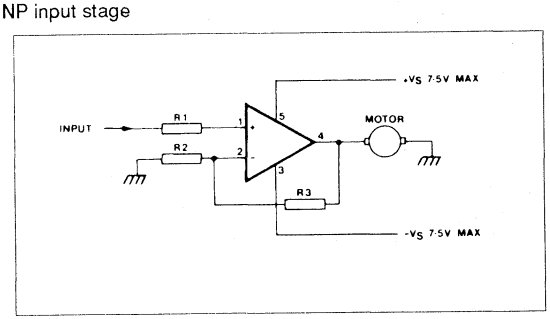


Fig. 4 SL6310 servo amplifier

OPERATING NOTES

Mute facility

The SL6310 has two mute control pins to allow easy interfacing to inputs of high or low levels. Mute control 'A', pin 7, is left open circuit or connected to a voltage within 0.65 volt of Vcc (via a 100kΩ resistor) for normal operation. When the voltage on pin 7 is reduced to within 1 volt of earth (via a 100kΩ resistor) the SL6310 is muted

Audio amplifier

AstheSL6310 is an operational amplifier it is easy to obtain the voltage gain and frequency response required. To keep the input impedance high it is wise to feed the signal to the non-inverting input as shown in Fig.2. In this example the input impedance is approximately 100kΩ. The voltage gain is determined by the ratio (R3 + R4)/R3 and should be between 3 and 30 for best results. The capacitor in series with R3, together with the input and output coupling capacitors, determines the low frequency rolloff point. The upper frequency limit is set by the device but can be restricted by connecting a capacitor across R4.

Operational amplifier

It is impossible to list all the application possibilities in a single data sheet but the SL6310 offers considerable advantages over conventional devices in high output current applications such as lamp drivers (Fig.3) and servo amplifiers (Fig.4) .

Buffer and output stages for signal generators are another possibility together with active filter sections requiring high output current.

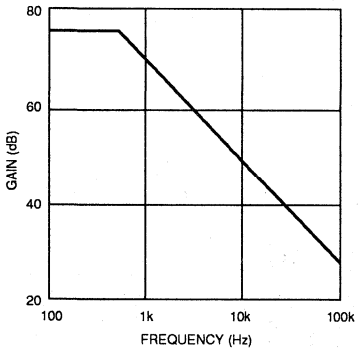


Fig. 5 Gain v. frequency

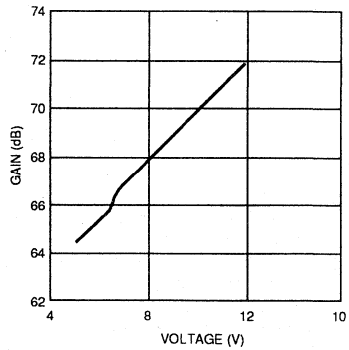


Fig. 6 Gain v. supply voltage

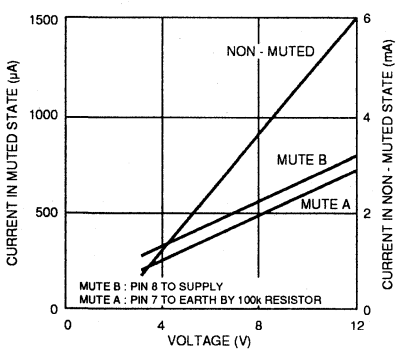


Fig. 7 Supply current v. supply voltage

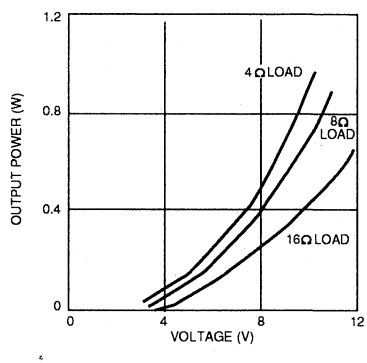


Fig. 8 Output power v. supply voltage at 5% (max) distortion

DS3047-2.3

SL6442

1GHZ AMPLIFIER/MIXER

(Supersedes June 1991 Edition)

The SL6442 EHF Amplifier and Mixer is designed for use in cordless telephones, cellular telephones, pagers and low-power receivers operating at frequencies up to 1GHz. It contains a low noise amplifier (LNA) with AGC facility and two mixers for use in I and Q direct conversion receivers or image cancelling in superheterodyne receivers.

Operating from a single supply of 5V, the SL6442 requires a current of 4.6mA (typ.) when powered up and only 11µA (typ.) when powered down using the battery economy facility.

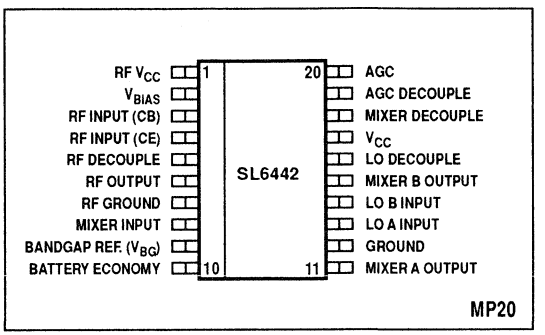


Fig.1 Pin connections - top view

FEATURES

- 1GHz Operation
- Very Low Power
- Suitable for Direct Conversion or Superhet Systems
- On-Chip RF Amplifier
- Power Down Facility for Battery Economy
- AGC Capability

ORDERING INFORMATION

SL6442 NA MP Miniature Plastic DIL Package

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	–55°C to +150°C
Operating temperature	0°C to +70°C

This device has highly static-sensitive terminations, sensitivity measured as typically 700V using MIL-STD-883 Method 3015. Therefore, ESD handling precautions are essential in order to avoid degradation of performance or permanent damage to the device.

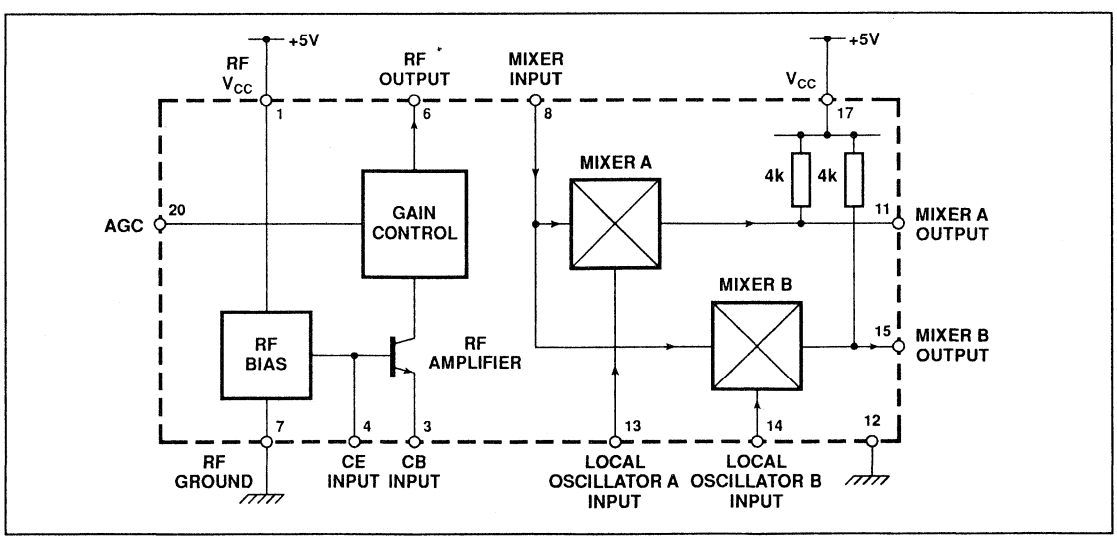


Fig.2 block diagram

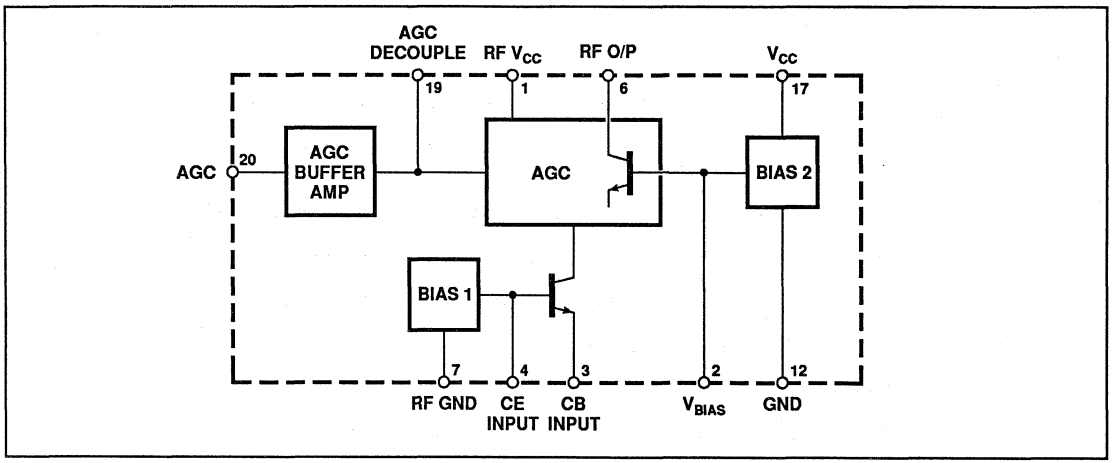


Fig.3 Circuit schematic of LNA

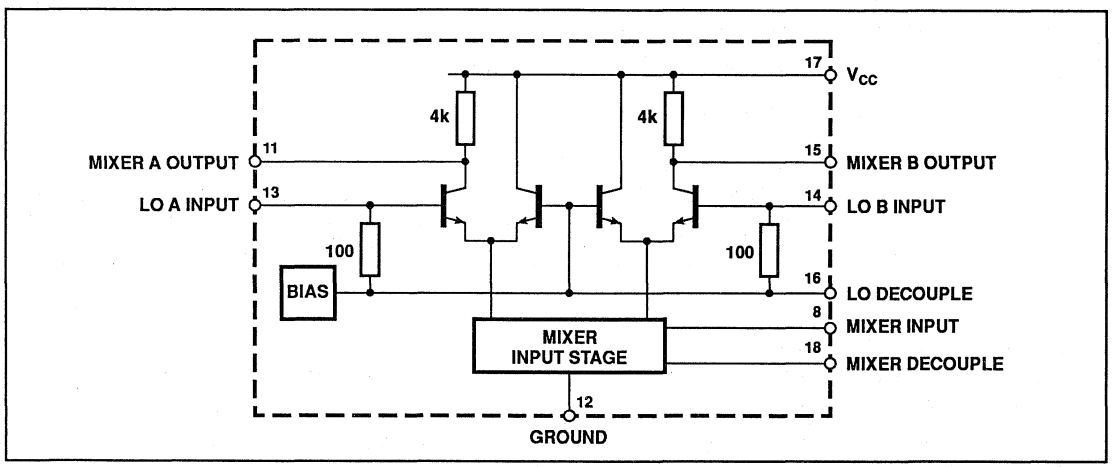


Fig.4 Circuit schematic of mixer

PIN DESCRIPTIONS

Pin no.	Name	Description
1	RF V_{CC}	Power supply to the RF amplifier. Normally connected to +5V, it should be adequately bypassed.
2	V_{BIAS}	A 1·6V bias source capable of supplying up to 0·5mA.
3	RF input (CB)	Common base input to the emitter of the RF transistor. It should be returned to ground for DC using an RF choke or tuned circuit when in common base mode. In common emitter mode it should be connected directly to ground.
4	RF input (CE)	Common emitter input to the base of the RF transistor. It is DC biased internally but should be decoupled in common base mode.
5	RF decouple	Decoupling of DC bias line.
6	RF output	Output port of the RF amplifier. It should be returned to +5V via an RF load. A current of 2mA will flow if pin 20 (AGC) is connected to pin 9 (V_{BG}).

PIN DESCRIPTIONS (Continued)

Pin no.	Name	Description
7	RF ground	A separate ground is provided for the RF amplifier to improve stability.
8	Mixer input	This is coupled externally to the output of the RF amplifier (pin 6). It should be decoupled to V_{BIAS} via an RF choke.
9	Bandgap ref. (V_{BG})	Temperature compensated DC reference voltage. It should not be loaded.
10	Battery economy	Turns device 'off' when HIGH (>3V), 'on' when LOW (<1·5V).
11	Mixer A output	The output impedance is about 4kΩ; quiescent voltage is approximately 4V (V_{CC}=5V).
12	Ground	Mixer and biasing ground.
13	Local osc. A input	Input level of –10dBm. DC level is approximately 2·3V.
14	Local osc. B input	Input level of –10dBm. DC level is approximately 2·3V.
15	Mixer B output	The output impedance is about 4kΩ; quiescent voltage is approximately 4V (V_{CC}=5V).
16	LO decouple	Decoupling of DC bias line.
17	V_{CC}	+5V supply; it should be bypassed effectively.
18	Mixer decouple	Decoupling of DC bias line.
19	AGC decouple	Decoupling of AGC input line.
20	AGC	Varies RF amplifier gain. Gain reduces with increasing voltage, with RF gain reduced by 6dB when AGC=V_{BIAS}. Full range of AGC requires only typically 300mV DC range (see Fig. 6). This pin should be connected to V_{BG} if the AGC facility is not required.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated:

T_{AMB}=25°C, V_{CC}=4·5V and at V_{CC}=6·5V

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Total supply current	1, 6, 11, 15, 17	3·5	4·6	5·5	mA	Pin 10 at 0V
Total supply current (economised)	1, 6, 11, 15, 17		11·0	15·0	µA	Pin 10 at V_{CC}
Battery economiser input current	10	–1·0		1·0	µA	
Total RF amplifier current	1, 5	1·75		2·75	mA	
Maximum RF amplifier current	6			2·75	mA	V_{AGC}=1·2V
Minimum RF amplifier current	6			10·0	µA	V_{AGC}=2·0V
AGC amplifier offset voltage	20, 19	–20·0		+20·0	mV	
Bandgap voltage, V_{BG}	9	1·00	1·22	1·40	V	
V_{BIAS}	2	1·40	1·64	1·80	V	
V_{BIAS} supply regulation	2		+24·0	+50	mV	Step V_{CC} from 4·50V to 5·50V,
V_{BIAS} load regulation	2		–17·0	–50	mV	Step load from 0mA to 0·5mA,
Mixer conversion gain	11, 15	10·0	12·7	16·0	dB	$f_{CARRIER}$=50MHz at –10dBm, f_{SIGNAL}=50·01MHz at –34dBm, IF=10kHz, Z_L (EXT)=1MΩ//20pF
Mixer A/B gain match	11, 15	–1·0	0	+1·0	dB	$f_{CARRIER}$=50MHz at –10dBm, f_{SIGNAL}=50·01MHz at –34dBm, IF=10kHz, Z_L (EXT)=1MΩ//20pF

ELECTRICAL CHARACTERISTICS OF THE SL6442 DEMONSTRATION BOARD (PAGES 6-9)

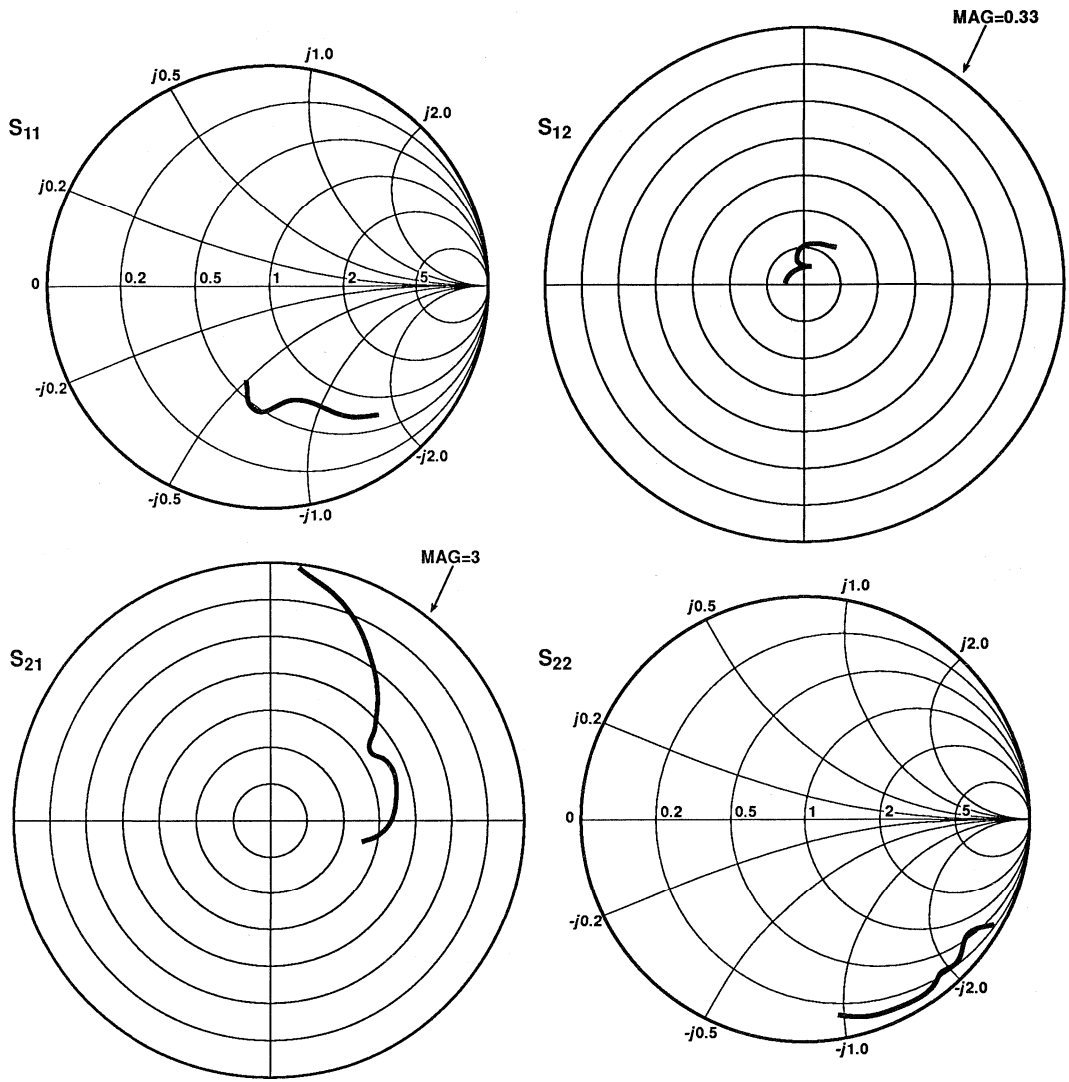
These characteristics are guaranteed over the following conditions unless otherwise stated.

T_{AMB} = 25° C, V_{CC} =5·0V, V_{AGC} = V_{BG}, LO = –5dBm, Input/Output = 50Ω, f_{IN} = 950MHz, f_{LO} = 930MHz (IF = 20MHz), f_{LO} = 949·990MHz (IF = 10kHz)

Overall performance	Typ.	Units	Conditions
Noise figure	8·2	dB	DSB (20MHz IF)
Third order input intercept	–22	dBm	20MHz IF
Power gain	7	dB	20MHz IF
Voltage gain	30	dB	Z_L > 100kΩ IF = 10kHz

SUPPLEMENTARY INFORMATION

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Operating supply voltage range		4·5	5·0	6·5	V	
RF Amplifier Common emitter						
Power gain			14		dB	Matched input and output.
AGC range	20		25		dB	V_{BIAS} ±150mV typ. (see Fig. 6).
Input intercept			–9		dBm	Third order.
1dB gain compression			–23		dBm	
Noise figure			4·5		dB	Common emitter.
Input impedance						See Fig. 5.
Optimum operating frequency range	4	400		1000	MHz	
Mixers (950MHz)						
Voltage conversion gain			19		dB	At IF = 50kHz, matched input.
Power conversion gain			–7		dB	At IF = 20kHz. Matched input and output.
LO drive level	13,14		–10		dBm	Measured at pins 13 and 14.
Input intercept point	8		–6		dBm	Third order.
1dB gain compression			–12		dBm	
Mixer 'A' to Mixer 'B' gain input match				±1·0	dB	Equal LO level at pins 13 and 14
Mixer 'A' to Mixer 'B' phase input match				±4	deg	LO inputs 90 ± 0·1° phase
Input impedance						See Fig. 7.
Noise figure			21		dB	
Optimum operating frequency range	8			1000	MHz	Low frequency operation dependent on external components.
IF output bandwidth	11,15		20		MHz	Can be extended by external tuned circuit.
Output impedance			4		kΩ	
Isolation LO to mix RF I/P		25			dB	All ports terminated with 50Ω
Reverse isolation of RF amp		14			dB	All ports terminated with 50Ω
Isolation LO to IF		50			dB	All ports terminated with 50Ω
Isolation RF to IF		37			dB	All ports terminated with 50Ω



	S_{11}		S_{12}		S_{22}		S_{21}	
Freq.(MHz)	Mag.	Ang.(°)	Mag.	Ang.(°)	Mag.	Ang.(°)	Mag.	Ang.(°)
400	0·70	–52	0·013	175	0·97	–30	3·49	94
500	0·61	–61	0·019	103	0·90	–36	2·90	83
600	0·55	–65	0·026	78	0·90	–40	2·57	71
700	0·53	–70	0·031	84	0·90	–44	2·24	59
800	0·52	–75	0·028	76	0·91	–50	1·99	49
900	0·51	–79	0·024	83	0·90	–55	1·79	41
1000	0·50	–82	0·028	60	0·91	–59	1·64	34
1100	0·53	–88	0·019	98	0·93	–66	1·71	27
1200	0·54	–100	0·038	95	0·94	–74	1·73	10
1300	0·47	–110	0·055	82	0·91	–83	1·47	–8
1400	0·41	–115	0·061	63	0·86	–90	1·26	–18

Fig.5 RF amplifier common emitter S-parameters

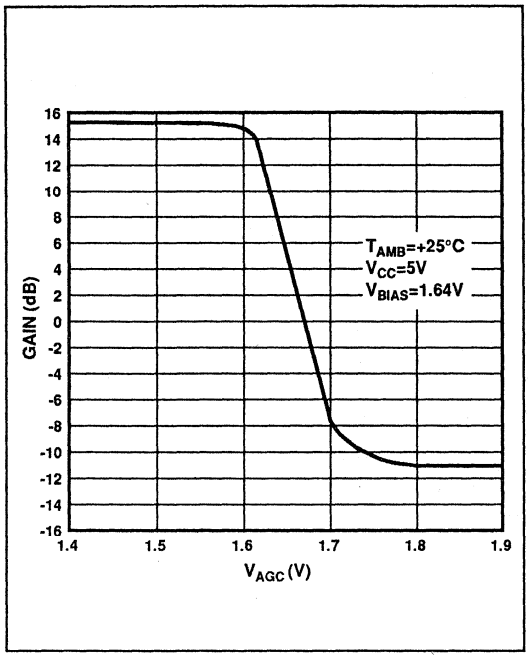
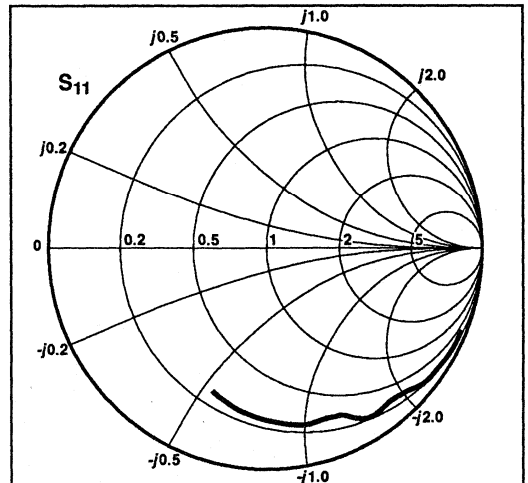


Fig.6 SL6442 AGC characteristic



Freq.(MHz)	Mag.	Ang.(°)	Freq.(MHz)	Mag.	Ang.(°)
400	0·99	–12	1000	0·81	–78
500	0·97	–26	1100	0·79	–88
600	0·96	–39	1200	0·76	–98
700	0·92	–51	1300	0·73	–108
800	0·88	–62	1400	0·66	–118
900	0·83	–70			

Fig.7 Mixer RF input impedance, S_{11} (pin 8)

APPLICATION CIRCUIT FOR USE AT 950MHz

This Application Note describes a circuit which demonstrates the functions and performance of the SL6442 in a 950MHz amplifier/mixer receiver front end configuration.

Fig. 8 is a schematic diagram which illustrates the arrangement of the ancillary components required for optimum performance at 950MHz. Component layout, PCB track and ground plane are shown in Figs. 9, 10 and 11, respectively. Approximate starting values for the components were obtained using Smith charts and data derived from S-parameter analysis (see Figs. 5 and 7).

The actual component values were determined by using a linear circuit simulator such as Touchstone™. In this case the circuit is optimised for maximum gain and minimum input reflection coefficient at the required frequency.

The input match is achieved using a stripline shorted-stub network. The LNA output to mixer input match is achieved by using a series inductor, and the mixer output to 50Ω match consists of a tunable LC network.

To prevent possible RF instability, pin 2 (V_{BIAS}) is decoupled with a series RC network as well as a 2·2µF capacitor. The quadrature phase shift components consist of phase lead (R3, C18) and phase lag (R2, C17) networks, which are capacitively coupled to the LO input pins. Inductor L3 serves to resonate out the parasitic capacitance between the two ports.

The exact values of the phase shift components were determined empirically and achieve a maximum amplitude and phase imbalance of about 1dB and 4 degrees respectively.

The variable capacitors VC1 and VC2 are adjusted to give a maximum output level at an IF of 20MHz. Other intermediate frequencies may require different values of VC1 and VC2 and/or L4 and L5. At zero IF, as in direct conversion receivers, the output matching network is transparent.

If the AGC facility is not required it is necessary to connect pin 20 to pin 9 (V_{BG}). The battery economy pin (10) may be connected directly to ground if the power down facility is not required.

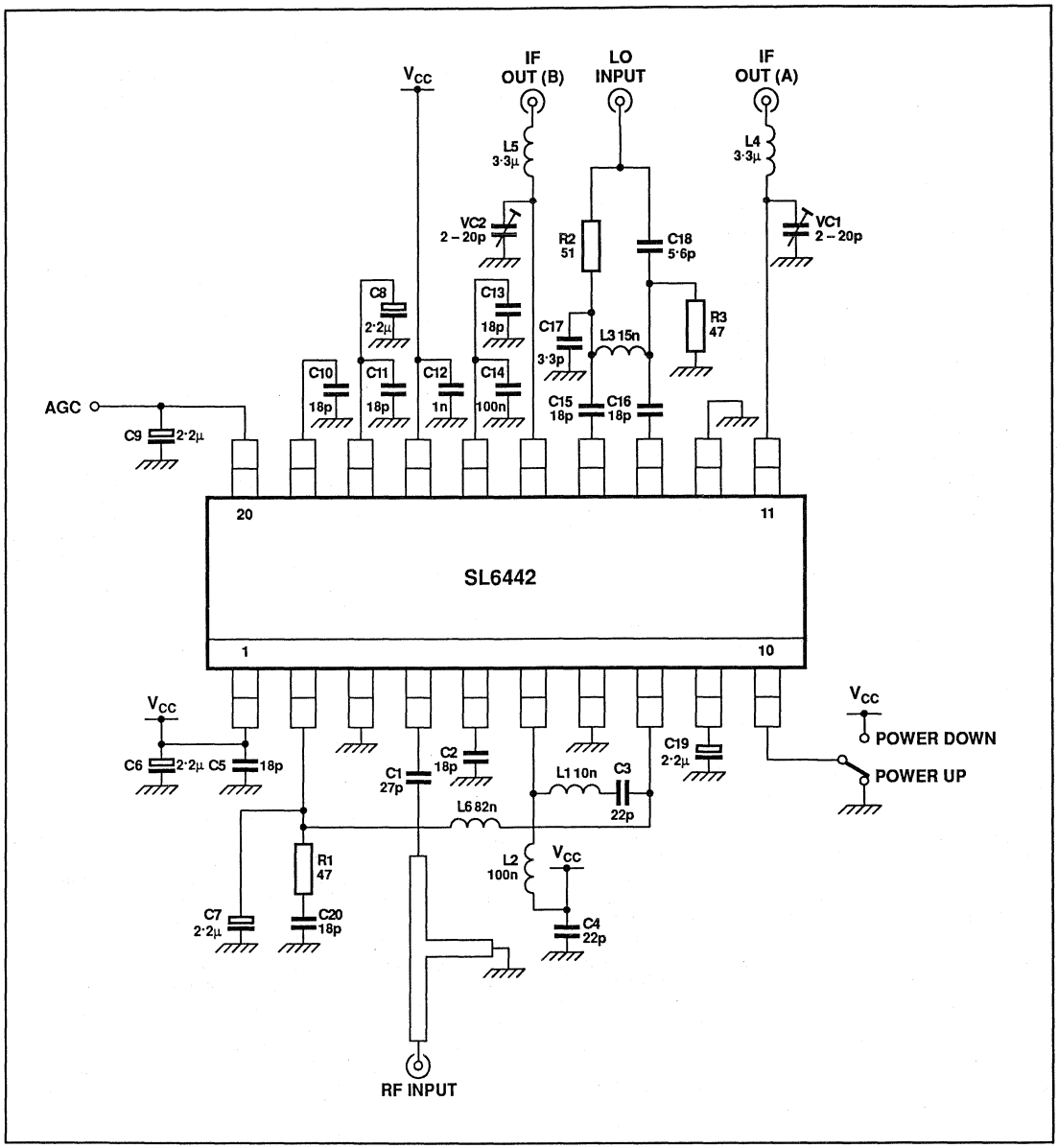
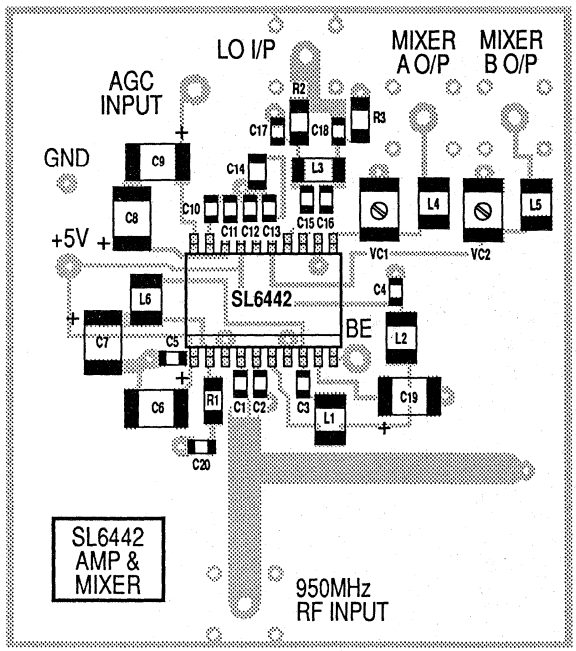


Fig.8 SL6442 demonstration board circuit



COMPONENT LIST

R1, R3	47Ω
R2	51Ω
C1	27pF
C2,C5,C10, C11,C13, C15	18pF
C3, C4, C6, C7,C8	22pF
C9, C19	2·2µF
C12	1nF
C14	100nF
C17	3·3pF
C18	5·6pF
L1	10nH
L2	100nH
L3	15nH
L4, L5	3·3µH
L6	82nH
VC1, VC2	2 - 20pF

Fig.9 SL6442 demonstration board component layout. Scale=2 x full size. Input and output coaxial connectors are mounted on the ground plane side of the board.

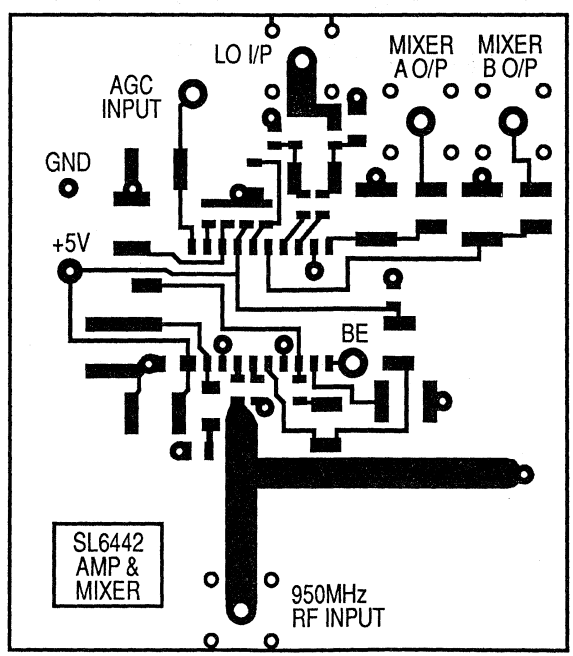


Fig.10 SL6442 demonstration board track. Scale=2 x full size

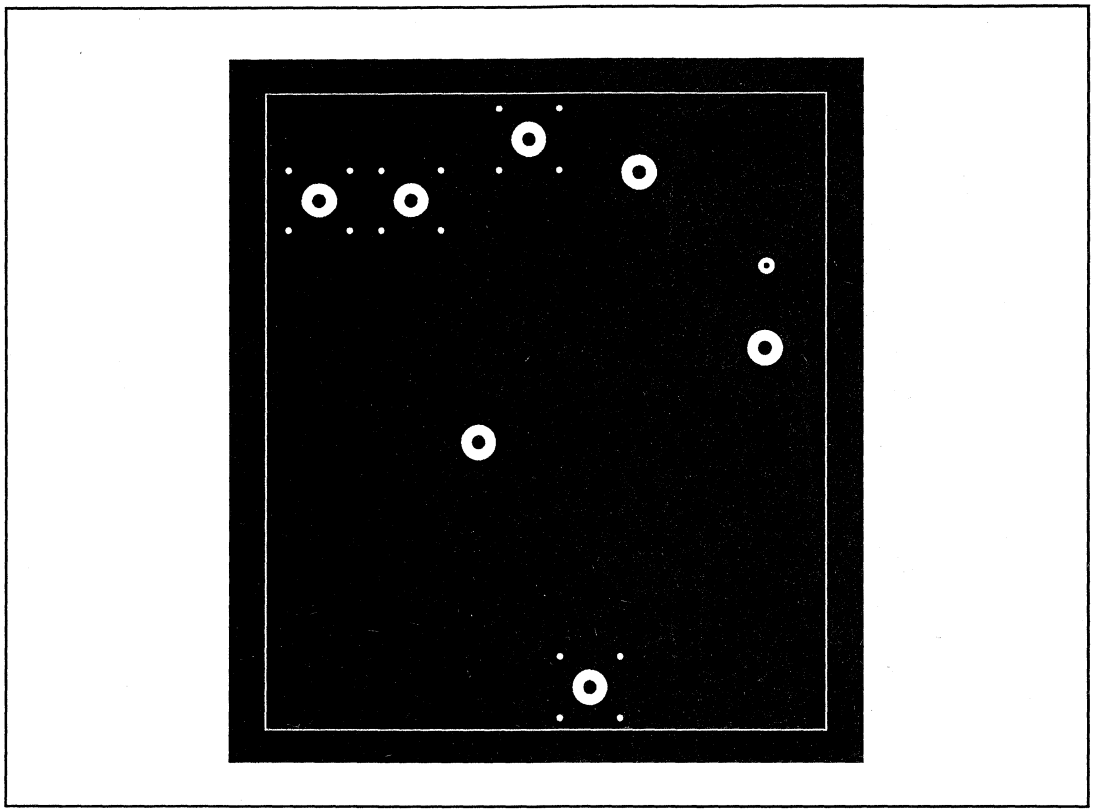


Fig.11 SL6442 demonstration board ground plane. Scale=2 x full size.

DS3224 1.8

SL6444

1GHz AMPLIFIER / MIXER

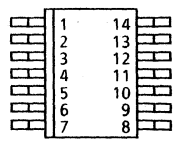
The SL6444 Amplifier and Mixer is designed for use in Cordless Telephones, Cellular Radios, Pagers, and Low Power receivers operating at frequencies up to 1GHz. It contains a low noise amplifier and mixer. Operating from a single supply it draws a current of 9.5mA and has a power down facility.

FEATURES

- 1GHz Operation
- Low Power Consumption
- Low Noise Figure
- Suitable for Superheterodyne Architectures
- Power Down Facility for Battery Economy
- Balun for Balanced Mixer Drive

ORDERING INFORMATION

SL6444 KG MPAS Miniature Plastic Dil Package



MP14

Pin	Function	Pin	Function
1	Battery Economy	14	Bandgap Ref.
2	Bias Supply	13	LO Input
3	RF Input	12	Ground
4	RF Ground	11	Mixer Output 180°
5	VCC decouple	10	Mixer Output 0°
6	RF Output	9	Mixer Current
7	VCC	8	Mixer Input

Fig.1 Pin connections - top view

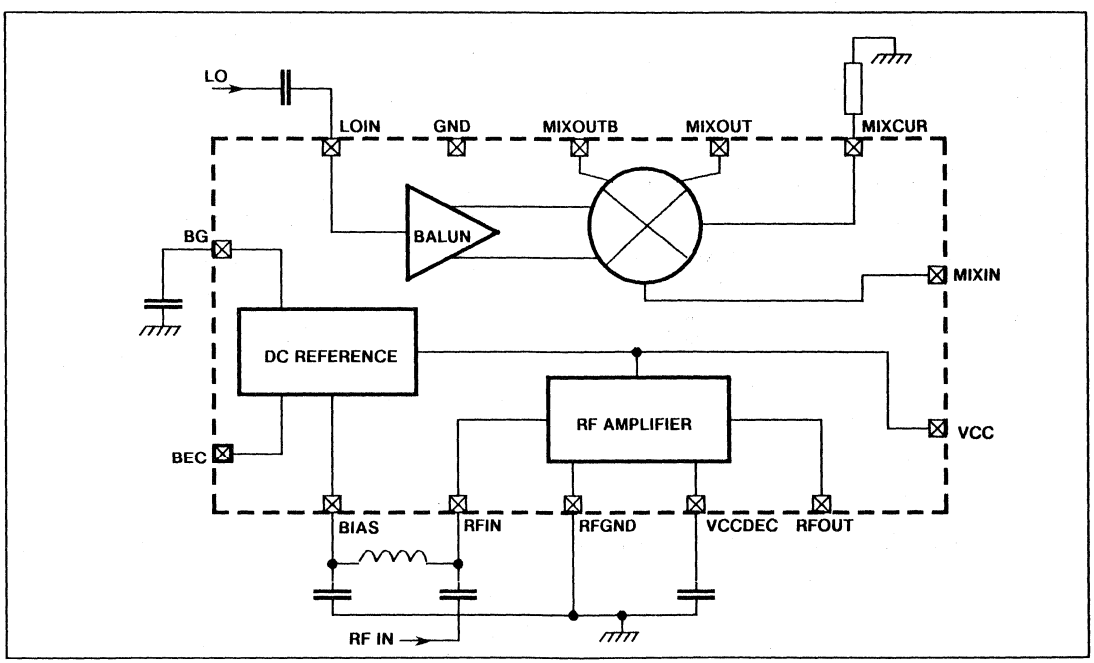


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated.
$T_{amb} = 25°C$, $V_{CC} = 5V$

NOTE. To acheive low noise performance, device structures used in this device mean that this device has static sensitive terminations, sensitivity typically measured as 200V using MIL-STD-883 method 3015. ESD handling precautions are essential to avoid degradation of performance or permanent damage to this device.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
DC CHARACTERISTICS						
Supply voltage	V_{CC}	2.7	5.0	6.0	V	
Supply current, I_{CC} Note 1			9.4		mA	Battery economy low
				0.5	µA	Battery economy high
Bandgap reference	VBG		1.23		V	No external load
Battery economy high	BEC	V_{CC}-0.5		V_{CC}	V	
Battery economy low	BEC	0		0.5	V	
Battery economy sink current	BEC			0.1	µA	Battery economy high
Battery economy source current	BEC			1.5	µA	Battery economy low
RF AMPLIFIER (COMMON EMITTER)						
Supply current	RFOUT		2.2		mA	
Input impedance	RFIN					50Ω system See Fig.3
Output impedance	RFOUT					50Ω system See Fig.3
Gain (RF_{IN} to RF_{OUT})						50Ω system See Fig.3
Reverse isolation (RF_{OUT} to RF_{IN})						50Ω system See Fig.3
MIXER						
Optimum frequency range	MIXIN	0.1			GHz	
Supply current Note 2.			4.4		mA	
Input impedance	MIXIN					50Ω system See Fig.4
Output impedance	MIXOUT					50Ω system See Fig.4
	MIXOUTB					50Ω system See Fig.4
Mixer conversion voltage gain	MIXOUT MIXOUTB	9			dB	LOIN 100MHz -15dBm MIXIN 100.01MHz 470Ω loads at MIXOUT and MIXOUTB

NOTES: (1) Total device supply current
(2) Half mixer current in each of MIXOUT and MIXOUTB

PERFORMANCE CHARACTERISTICS (GPS Demonstration boards)

Test conditions (unless otherwise stated): VCC = 5V; T_{amb} = 25°C
Input frequency 915MHz; Local oscillator frequency 765MHz;
Intermediate frequency 150MHz; Local oscillator amplitude 80mV r.m.s.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
RF AMPLIFIER COMMON EMITTER (Note 1)						Application circuit Fig. 5
Power gain			18		dB	
Third order intercept point			-12		dBm	At input
Noise figure			2.7		dB	
Output power at 1dB gain compression			-6		dBm	
SINGLE BALANCED MIXER (Note 1)						Application circuit Fig. 6
Power conversion gain			8.6		dB	
Third order intercept point			-4.5		dBm	At input
Double sideband noise figure			9.7		dB	
LO to RF isolation			28		dB	
LO to IF isolation			39		dB	
RF to IF isolation			18		dB	
DOUBLE BALANCED MIXER (Note 1)						Application circuit Fig. 7
Power conversion gain			13			
Third order intercept point			-7		dBm	At input
Double sideband noise figure			9.7		dB	
LO to RF isolation			26		dB	
LO to IF isolation			42		dB	
RF to IF isolation			32		dB	

NOTE .

1. Application circuit has been optimised for minimum noise figure and maximum gain.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55°C to + 150°C
Operating temperature	-10°C to + 85°C

PIN NO	NAME	TITLE	DESCRIPTION
1	BEC	Battery Economy	Turns device off when "HIGH", on when "LOW".
2	BIAS	Bias Supply	Controls the bias current in the RF amplifier. Must be decoupled externally to ground through 1nf capacitor.
3	RFIN	RF Input	This is the common emitter input to the base of the RF transistor. It is DC biased externally through a suitable inductor to the bias pin, pin 2.
4	RFGND	R.F. Ground	Must be connected to the system ground with minimum inductance
5	VCCDEC	VCC Decouple	This pin allows the VCC supply at the RF Amplifier to be effectively decoupled.
6	RFOUT	RF Output	The collector of the RF amplifier output transistor. Must be returned to VCC through a load in which the DC bias current can flow.
7	VCC	Power Supply	Positive supply
8	MIXIN	Mixer Input	Input port of mixer, should be AC coupled externally.
9	MIXCUR	Mixer Current	A resistor may be placed between this pin and ground to reduce mixer current. Otherwise connect to GND.
10	MIXOUT	Mixer Output 0°	Output port of the mixer An open collector output which must be returned to VCC through a suitable load. Half of the total Mixer current will flow from this port.
11	MIXOUTB	Mixer Output 180°	Output port of the mixer. An open collector output which must be returned to VCC through a suitable load. Half the total mixer current will flow from this port.
12	GND	Ground	Must be connected to the system ground with minimum inductance
13	LOIN	LO Input	Local Oscillator input to mixer, should be AC coupled externally.
14	VBG	Bandgap	Temperature compensated voltage reference. Must be decoupled externally to ground through a 1nF capacitor

VCC = 5V Amplifier current 2.2mA

FREQ-MHz	MAG [S11]	ANG [S11]	MAG [S21]	ANG [S21]	MAG [S12]	ANG [12]	MAG [S22]	ANG [S22]
100.000	0.91	-10	5.89	167	0.016	158	0.99	-5
200.000	0.89	-21	5.86	151	0.010	-75	0.99	-11
300.000	0.86	-30	5.60	136	0.004	55	0.99	-16
400.000	0.81	-39	5.19	121	0.003	118	0.98	-21
500.000	0.77	-47	4.86	108	0.004	-102	0.97	-25
600.000	0.72	-55	4.48	95	0.005	154	0.98	-32
700.000	0.67	-63	4.11	84	0.004	134	0.97	-38
800.000	0.62	-70	3.73	73	0.008	165	0.97	-44
900.000	0.58	-77	3.35	61	0.008	150	0.94	-52
1000.00	0.55	-83	2.97	52	0.010	117	0.91	-59
1100.00	0.52	-87	2.64	43	0.014	97	0.87	-66
1200.00	0.49	-92	2.32	34	0.013	82	0.82	-73
1300.00	0.47	-95	2.06	28	0.010	78	0.76	-79
1400.00	0.45	-98	1.85	22	0.009	59	0.71	-85
1500.00	0.45	-101	1.71	16	0.004	80	0.67	-89

SL6444 Typical RF Amplifer scattering parameters

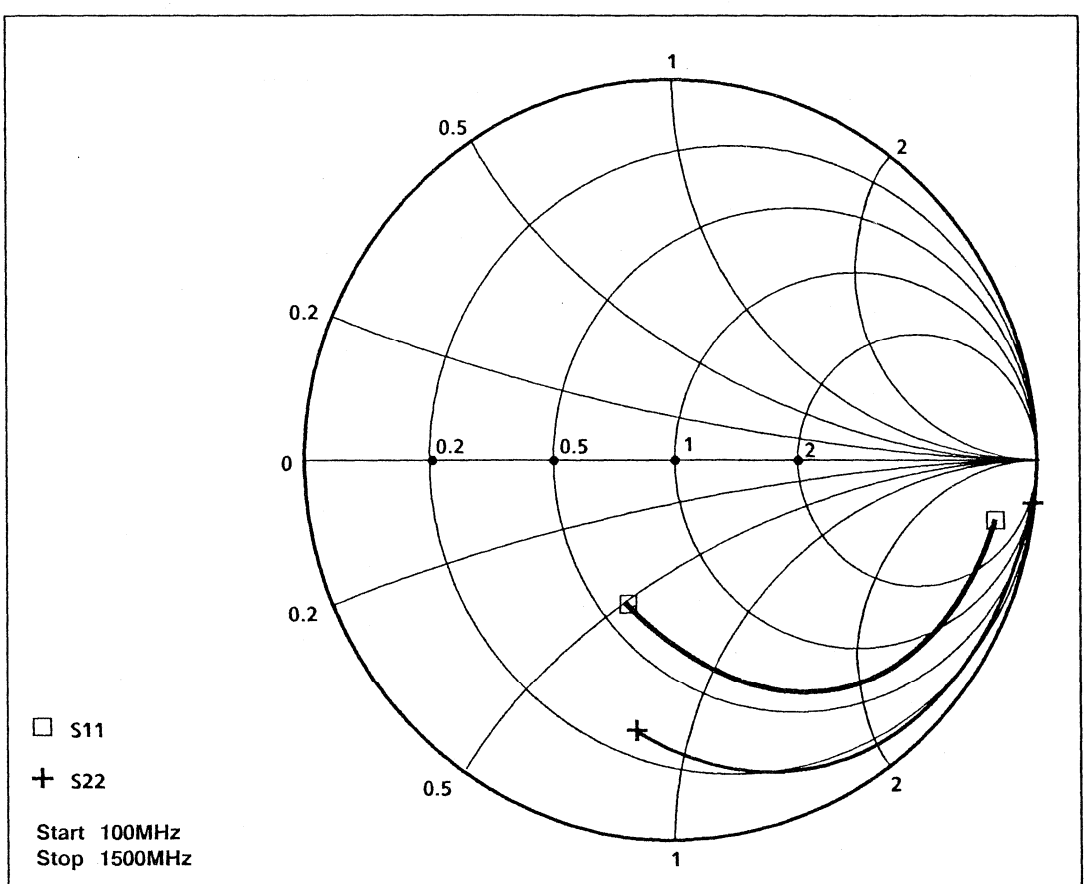


Fig. 3 Typical Input and Output Impedance of SL6444 RF Amplifier (Normalised to 50Ω)

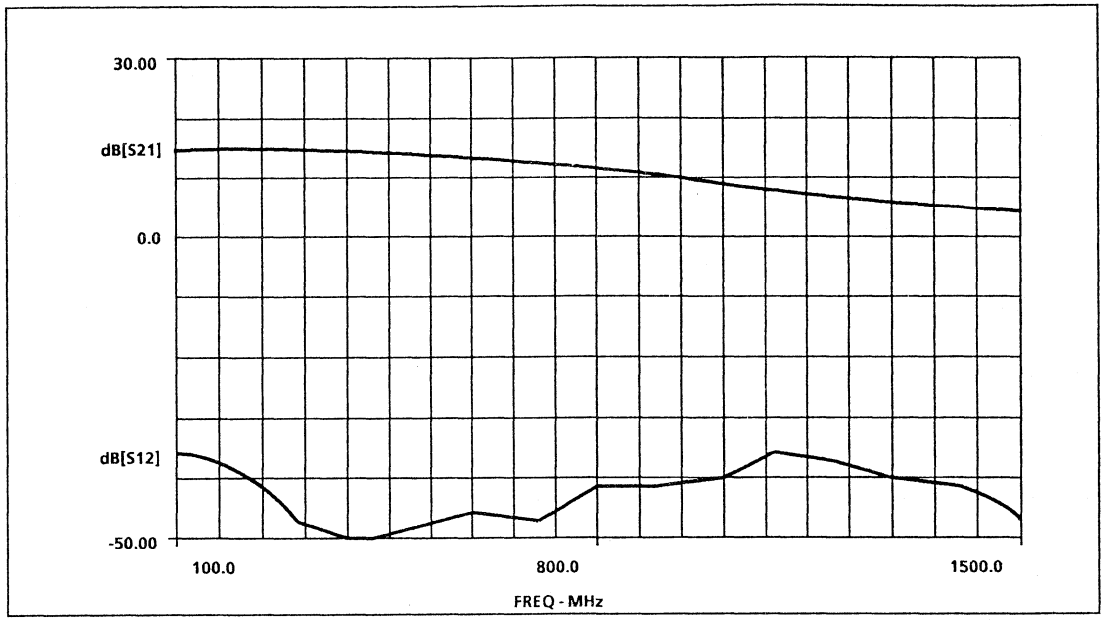


Fig. 3b Typical gain and reverse isolation of SL6444 RF Amplifier in a 50 Ohm test system.

VCC = 5V Mixer current 4.4mA S22 is measured at either MIXOUT or MIXOUTB S11 is measured at MIXIN

FREQ-MHz	MAG [S11]	ANG [S11]	MAG [S22]	ANG [S22]
100.000	0.79	-6	1.00	-6
200.000	0.78	-13	0.99	-12
300.000	0.77	-20	0.99	-16
400.000	0.76	-28	0.97	-22
500.000	0.77	-34	0.96	-28
600.000	0.78	-41	0.97	-35
700.000	0.73	-50	0.94	-40
800.000	0.70	-58	0.91	-47
900.000	0.68	-67	0.88	-54
1000.00	0.64	-76	0.86	-60
1100.00	0.61	-86	0.83	-67
1200.00	0.58	-95	0.79	-74
1300.00	0.55	-105	0.75	-82
1400.00	0.51	-117	0.71	-89
1500.00	0.49	-129	0.68	-9

SL6444 Typical Mixer port impedance

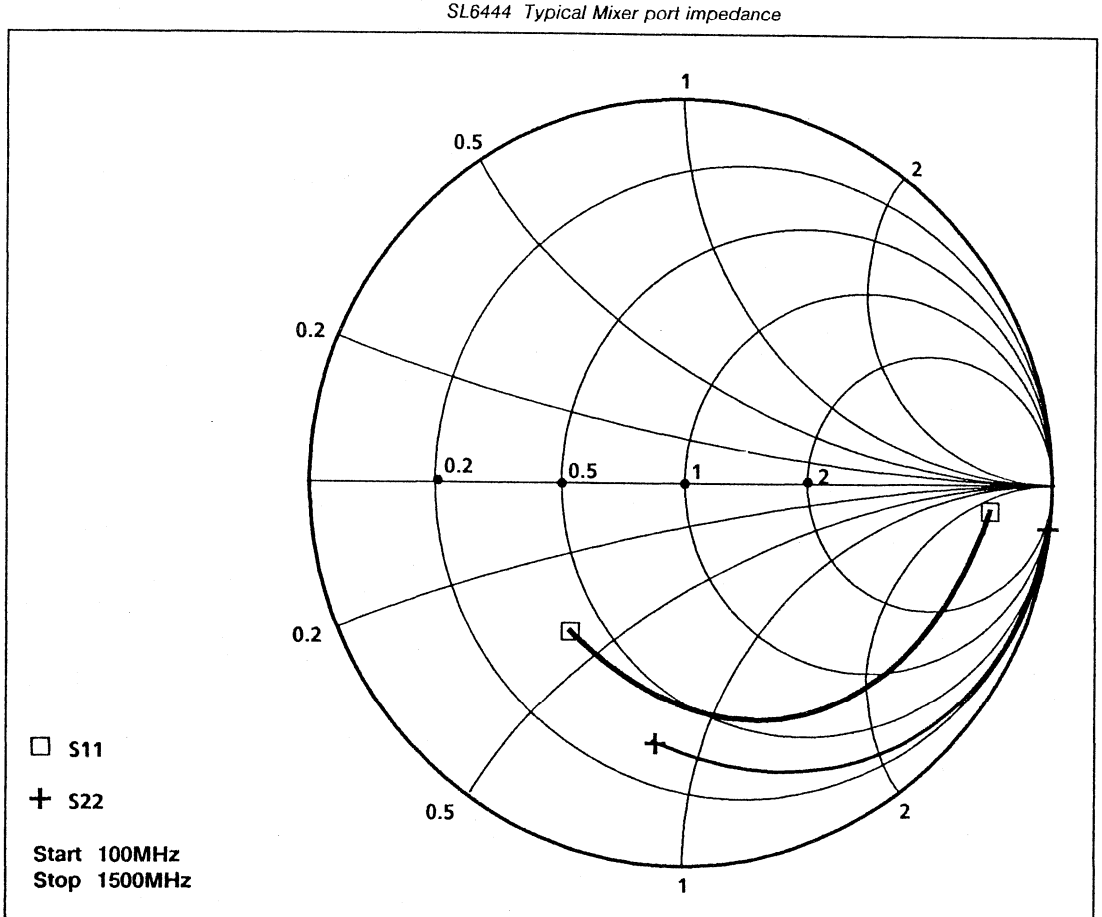
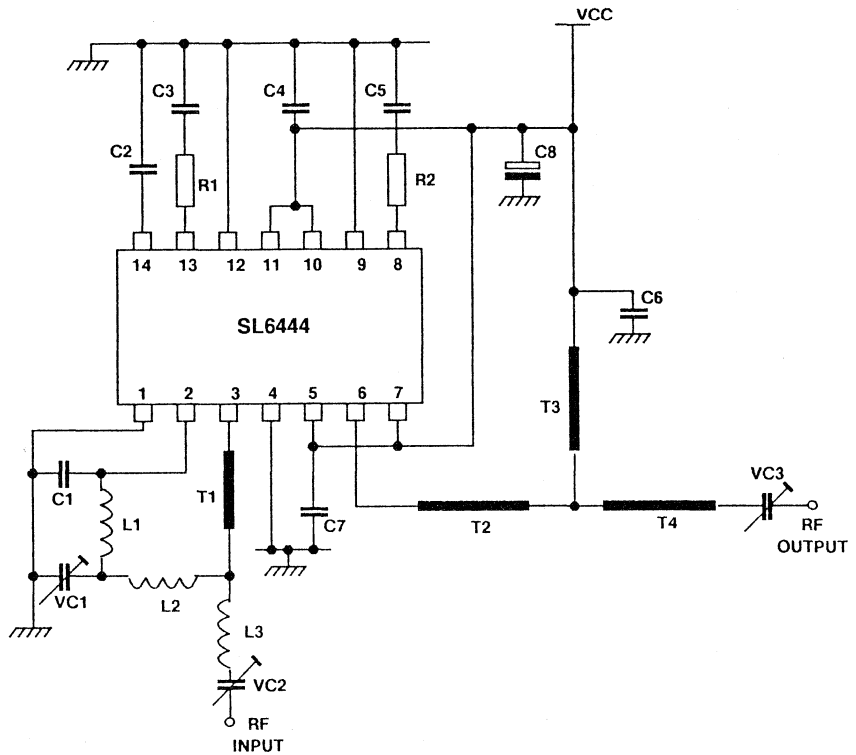


Fig. 4 Typical Input and Output Impedance of SL6444 Mixer
(Normalised to 50Ω)



NOTES

1. Double sided board should be used
2. Low inductive resistors should be used
3. Good quality capacitors with high self resonant frrequency should be used
4. Components should be placed in close proximity to device

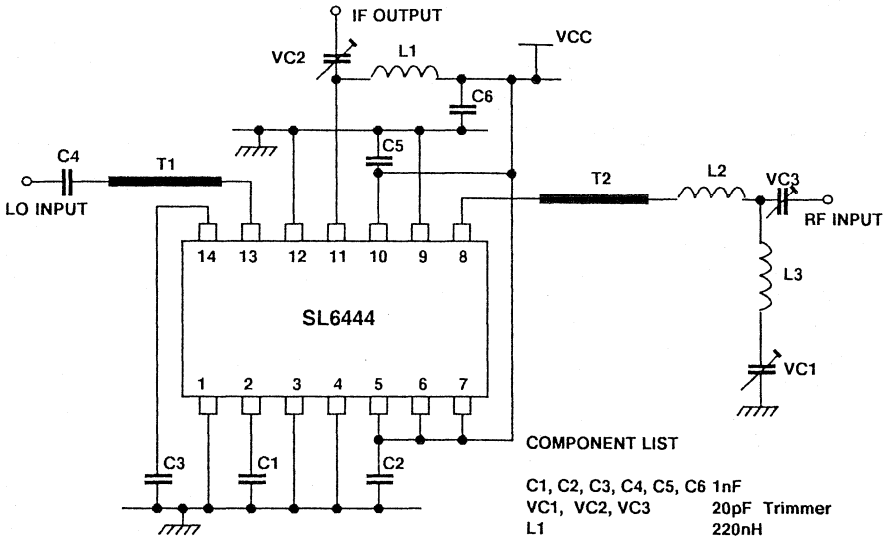
COMPONENT LIST

R1, R2	47 Ohm
C1, C2, C3, C4 C5, C7	1nF
C6	270pF
C8	1µF
VC1, VC2, VC3	20pF Trimmer
L1	56nH
L2	39nH
L3	6nH 1 Turn 24SWG 8mm diameter

Microstrip lines 0.5mm wide on 1.6mm thick glass fibre PCB and the following lengths.

T1	5mm
T2	16mm
T3	8mm
T4	15mm

Fig. 5 SL6444 RF amplifier demonstration circuit

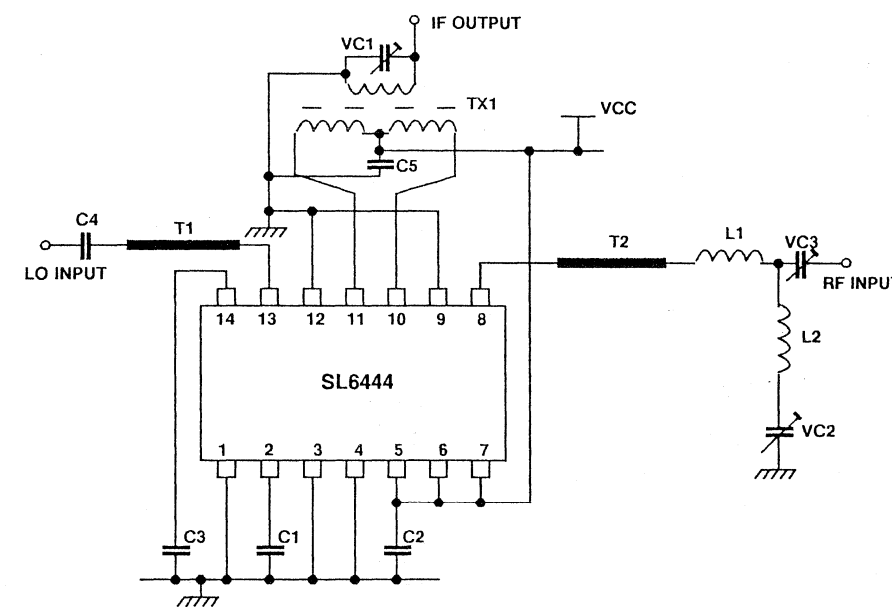


COMPONENT LIST

C1, C2, C3, C4, C5, C6	1nF
VC1, VC2, VC3	20pF Trimmer
L1	220nH
L2	6nH 1 Turn 24SWG 8mm diameter
L3	39nH
T1	50 Ohm line

Microstrip lines T2 is 0.5mm wide on 1.6mm thick glass fibre PCB and of length 5mm.

Fig. 6 Single balanced mixer demonstration circuit



COMPONENT LIST

C1, C2, C3, C4, C5	1nF	L1	6nH 1 Turn 24SWG 8mm diameter
VC1, VC2, VC3	20pF Trimmer	L2	39nH
		T1	50 Ohm line

TX1 4 + 4:1
Transformer wound on a 2.5mm long double aperture ferrite bead. The material having an initial permeability of approximately 15.

Microstrip lines T2 is 0.5mm wide on 1.6mm thick glass fiber PCB and of length 5mm.

Fig. 7 Double balanced mixer demonstration circuit

SL6601C

FM IF, PLL DETECTOR (DOUBLE CONVERSION) AND RF MIXER

The SL6601 is a straight through or single conversion IF amplifier and detector for FM radio applications. Its minimal power consumption makes it ideal for hand held and remote applications where battery conservation is important. Unlike many FM integrated circuits, the SL6601 uses an advanced phase locked loop detector capable of giving superior signal to-noise ratio with excellent co-channel interference rejection, and operates with an IF of less than IMHz. Normally the SL6601 will be fed with an input signal of up to 17MHz: there is a crystal oscillator and mixer for conversion to the IF amplifier, a PLL detector and squelch system.

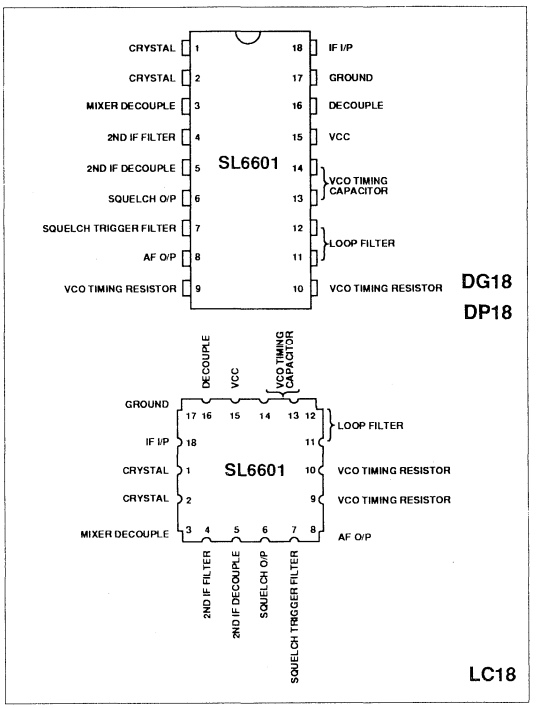


Fig. 1 Pin connections - top view

FEATURES

- High Sensitivity 2μV Typical
- Low Power: 2.3mA Typical at 7V
- Advanced PLL Detector
- Available in Miniature 'Chip Carrier' Package
- 100% Tested for SINAD

APPLICATIONS

- Low Power NBFM Receivers
- FSK Data Equipment
- Cellular Radio Telephones

QUICK REFERENCE DATA

- Supply Voltage 7V
- 50dB S/N Ratio

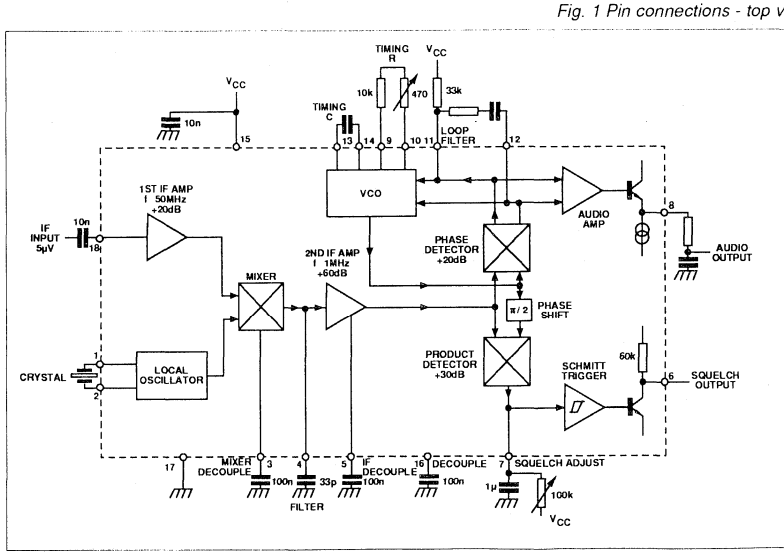


Fig. 2 SL6601 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC} : 7V
Input signal frequency: 10.7MHz, frequency modulated with a 1kHz tone with a ±2.5kHz frequency deviation
Ambient temperature: -30°C to +85°C; IF = 100kHz; AF bandwidth = 15kHz

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		2.3	2.7	mA	
Input impedance	100		300	Ω	Source impedance =200Ω
Input capacity	0.5	2.0	3.5	pF	
Maximum input voltage level	0.5			V rms	At pin 18
Sensitivity	5	2		µV rms	At pin 18 for S + N/N = 20dB
Audio output	35	90	140	mV rms	
Audio THD		1.3	3.0	%	1mV rms input at pin 18
S + N/N	30	50		dB	1mV rms input at pin 18
AM rejection	30	Note 1		dB	100µV rms input at pin 18, 30% AM
Squelch low level		0.2	0.5	V dc	20µV rms input at pin 18
Squelch high level	6.5	6.9		V dc	No input
Squelch hystersis		1	6	dB	3µV input at pin 18
Noise figure		6		dB	50Ω source
Conversion gain		30		dB	Pin 18 to pin 4
Input gain compression		100		µV rms	Pin 18 to pin 4, 1dB compression
Squelch output load	250			kΩ	
Input voltage range	80	100		dB	At pin 8; above 20dB S + N/N
3rd order intercept point (input)		-38		dBm	Input pin 18, output pin 4
VCO frequency					
Grade 1	85		100	kHz	390pF timing capacitor } No input
Grade 2	95		110	kHz	390pF timing capacitor } No input
Grade 3	105		120	kHz	390pF timing capacitor } No input
Source impedance (pin 4)		25	40	kΩ	
AF output impedance		4	10	kΩ	
Lock-in dynamic range	±8			kHz	20µV to 1mV rms at pin 18
External LO drive level	50		250	mV rms	At pin 2
Crystal ESR			25	Ω	10.8MHz

APPLICATION NOTES

IF Amplifiers and Mixer

The SL6601 can be operated either in a 'straight through' mode with a maximum recommended input frequency of 800kHz or in a single conversion mode with an input frequency of 50MHz maximum and an IF of 100kHz or ten times the peak deviation, whichever is the larger. The crystal oscillator frequency can be equal to either the sum or difference of the two IFs; the exact frequency is not critical.

The circuit is designed to use series resonant fundamental crystals between 1 and 17MHz.

When a suitable crystal frequency is not available a fundamental crystal of one third of that frequency may be used, with some degradation in performance.

E.G. If an external oscillator is used the recommended level is 70mV rms and the unused pin should be left O/C. The input is AC coupled via a 0.01µF capacitor.

A capacitor connected between pin 4 and ground will shunt the mixer output and limit the frequency response of the mixer output and limit the frequency response of the input signal to the second IF amplifier. A value of 33pF is advised when the second IF frequency is 100kHz; 6.8pF is advised for 455kHz.

Phase Locked Loop

The Phase Locked Loop detector features a voltage controlled oscillator with nominal frequency set by an external capacitor equal to (40 ±7)/f pF, where f is the VCO frequency in MHz The nominal frequency may differ from the theoretical but there is provision for a fine frequency adjustment by means of a variable resistor between the VCO output pins: a value of 470k has negligible effect while 6.8k (recommended minimum value) increases the frequency by approximately 20%.

Care should be taken to ensure that the free running VCO frequency is correct; because the VCO and limiting IF amplifier output produce square waves, it is possible to obtain lock with the VCO frequency fractionally related to the IF, e.g. IF = 100kHz, VCO = 150kHz. This condition can produce good SINAD ratios but poor squelch performance.

The loop filter is connected between pins 11 and 12; a 33k resistor is also required between pin 11 and Vcc.

The values of the filter resistor R2 and capacitor C1 must be chosen so that the natural loop frequency and damping factor are suitable for the FM deviation and modulation bandwidth required. The recommended values for various conditions are tabulated below:

Centre frequency kHz	Deviation kHz	Resistor kΩ	Capacitor pF
100	5	6.2	2200
100	10	5.6	1800
455	5	4.7	1500
455	10	3.9	1200

Note that the values of loop filter are not critical and in many cases may be omitted.

The AF output voltage depends upon the % deviation and so, for a given deviation, output is inversely proportional to centre frequency. As the noise is constant, the signal to noise ratio is also inversely proportional to centre frequency.

VCO Frequency Grading

The SL6601 is supplied in 3 selections of VCO centre frequency. This frequency is measured with a 390pF timing capacitor and no input signal.

Devices are coded 'SL6601 C' and a '/1','/2','/3' to indicate the selection.

Frequency tolerances are:

/1 85 - 100kHz (or uncoded)
/2 95 - 110kHz
/3 105 - 120kHz

Note that orders cannot be accepted for any particular selection, but all devices in a tube will be the same selection.

Squelch Facility

When inputs to the product detector differ in phase a series of current pulses will flow out of pin 7. The feature can be used to adjust the VCO; when a 1mV unmodulated input signal is applied to pin 18 the VCO frequency should be trimmed to maximise the voltage on pin 7.

The squelch level is adjusted by means of a preset variable resistor between pin 7 and Vcc to set the output signal to noise ratio at which it is required to mute the output. The capacitor between pin 7 and ground determines the squelch attack time. A value between 10nFand 10/1Fcan bechosento give the required characteristics.

Operation at signal to noise ratios outside the range 518dB is not recommended. Where the 'front end' noise is high (because of very high front end gain) the squelch may well never operate. This effect can be obviated by sensible receiver gain distribution.

The load on the squelch output (pin 6) should not be less than 250kΩ. Reduction of the load below this level leads to hysteresis problems in the squelch circuit.

The use of an external PNP transistor allows hysteresis to be increased. See Fig.4. The use of capacitors greater than 1000pF from pin 6 to ground is not recommended

Ouputs

High speed data outputs can be taken direct from pins 11 and 12 but normally for audio applications pin 8 is used A filter network will be needed to restrict the audio bandwidth and an RC network consisting of 4.7kn and 4.7nF may be used.

Layout Techniques and Alignment

The SL6601 is not critical in PCB layout requirements except in the 'straight through' mode. In this mode, the input components and circuits should be isolated from the VCO components, as otherwise the VCO will attempt to 'lock' to itself, and the ultimate signal to noise ratio will suffer.

The recommended method of VCO adjustment is with a frequency measurement system on pin 9. The impedance must be high, and the VCO frequency is adjusted with no input signal.

LOOP FILTER DESIGN

The design of loop filters in PLL detectors is a straight forward process. In the case of the SL6601 this part of the circuit is non-critical, and in any case will be affected by variations in internal device parameters. The major area of importance is in ensuring that the loop bandwidth is not so low as to allow unlocking of the loop with modulation.

Damping Factor can be chosen for maximum flatness of frequency response or for minimum noise bandwidth, and values between 0.5 and 0.8 are satisfactory, 0.5 giving minimum noise bandwidth.

Design starts with an arbitrary choise of fn, the natural loop frequency. By setting this at slightly higher than the maximum modulation frequency, the noise rejection can be slightly improved. The ratio fm/fn highest modulating frequency to loop frequency can then be evaluated.

From the graph, Fig.3 the value of the function

$$\frac{\Phi_{efN}}{\Delta f}$$

can be established for the desired damping factor.

Φ_e - peak phase error
f_n - loop natural frequency
Δf - maximum deviation of the input signal

and as f_n and Δf are known, Φ_e is easily calculated. Values for should be chosen such that the error in phase is between 0.5 and 1 radian. This is because the phase detector limits at $\pm\pi/2$ radians and is non linear approaching these points. Using a very small peak phase error means that the output from the phase detector is low, and thus impairs the signal to noise ratio. Thus the choice of a compromise value, and 0.5 to 1 radian is used. If the value of Φ_e achieved is far removed from this value, a new value of fn should be chosen and the process repeated.

With fn and D established, the time constants are derived from

$$t_1 + t_2 = \frac{K_O K_D}{(2\pi\, fn)^2}$$

$$\text{and } t_2 = \frac{D}{\pi\, FN} - \frac{1}{K_O K_D}$$

$K_O K_D$ is $0.3f_O$, where f_O is the operating frequency of the VCO. t_1 is fixed by the capacitor and an internal 20kΩ resistor: t_2 is fixed by the capacitor and external resistor.

$$\text{so } C = \frac{t_1}{2C \times 10^3}$$

$$\text{and } R_{ext} = \frac{t2 \times 20 \times 103}{2C \times 10^3}$$

In order that standard values may be used, it is better to establish a value of C and use the next lowest standard value e.g. C_{calc} = 238pF, use 220pF, as it is better to widen the loop bandwidth rather than narrow it.

The value of R_{ext} is then 'roundedup' by a similar process. It is, however, better to increase R_{ext} to the nearest preferred value as loop bandwidth is proportional $(R_{ext})^{1}/_{2}$ while damping factor is proportional to R: thus damping factor is increasing more quickly which gives a more level response.

Example

A frequency modulated signal has a deviation of 10kHz and a maximum modulating frequency of 5kHz. The VCO frequency is 200kHz.

Let f_n = 6kHz and D = 0.5

Then from the graph

$$\frac{\Phi_{efN}}{\Delta f} = 0.85$$

$$\Phi_e = \frac{0.85\Delta f}{f_n} = \frac{0.85 \times 10}{6} = 1.4 \text{ rads.}$$

This is too large, so increase f_n e.g. to 10kHz.

$$\frac{f_m}{f_n} = 0.5\frac{\Phi_{efN}}{\Delta f} = 0.45$$

$$\Phi_e = \frac{0.45 \times 10}{10} = 0.45$$

- which is somewhat low

Therefore set f_n = 7.5kHz

$$\frac{f_m}{f_n} = 0.666$$

$$\frac{\Phi_{efN}}{\Delta f} = 0.66$$

$$\Phi_e = \frac{0.66 \times 10}{7.5} = 0.88 \text{ rads.}$$

$$t_1 + t_2 = \frac{K_oK_D}{(2\pi fn)^2}$$

$K_oK_D = 0.3f_o$ where f_o is the VCO frequency

$$t_1 + t_2 = \frac{0.3 \times 200 \times 10^3}{(2\pi \times 7.5 \times 10^3)^2} = 27\mu S$$

$$t_2 = \frac{D}{\pi fn} - \frac{1}{K_oK_D}$$

$$= \frac{0.5}{\pi \times 7.5 \times 10^3} - \frac{1}{0.3 \times 200 \times 10^3}$$

$$= 4.5\mu S$$

$$t_1 = 22.5\mu S$$

$$C = \frac{t_1}{20 \times 10^3} = \frac{22.5 \times 10^{-6}}{20 \times 10^3} = 1.125nF \text{ (use 1nF)}$$

$$R = \frac{t_2}{t_1} \times 20 \times 10^3$$

$$= \frac{4.5}{22.5} \times 20 \times 10^3$$

$$= 4k\Omega \text{ (use 3.9K)}$$

Actual loop parameters can now be recalculated

t1 = 20µs t2 = 3.9µs

$$2\pi fn = \frac{(K_oK_D)}{(t_1 \times t_2} = \frac{(2 \times 10^5 \times 0.3)}{(23.9 \times 10^{-6})} = 50.1k \text{ rad/sec} = 7.97kHz$$

$$D = fn(t2 + \frac{1}{K_oK_D}) = \underline{0.515}$$

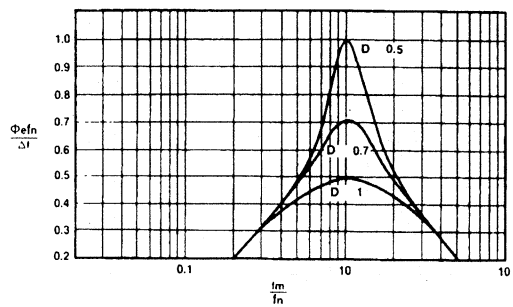


Fig. 3 Damping factor

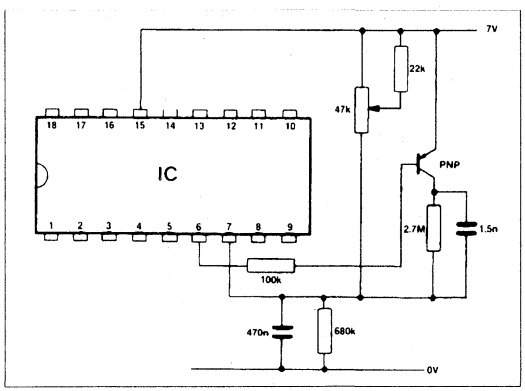


Fig. 4 Using an external PNP in squelch circuit

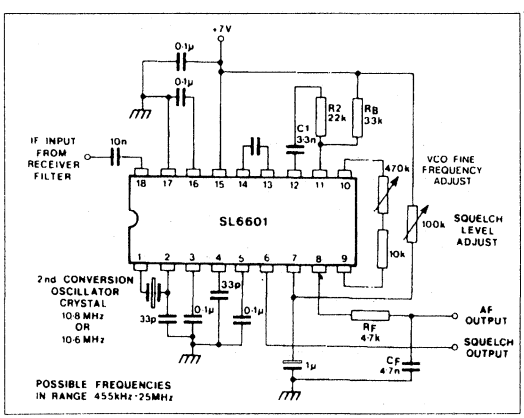


Fig. 5 SL6601 application diagram
(1st IF = 10.7MHz, 2nd IF = 100kHz)

TYPICAL CHARACTERISTICS

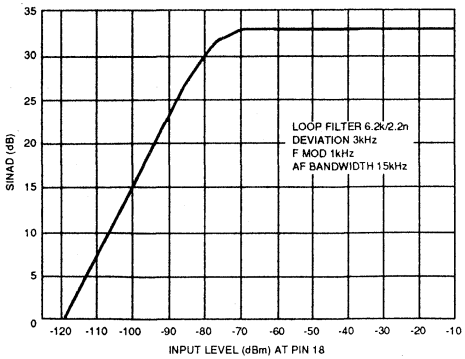


Fig. 6 Typical SINAD
(signal + noise + distortion/noise + distortion)

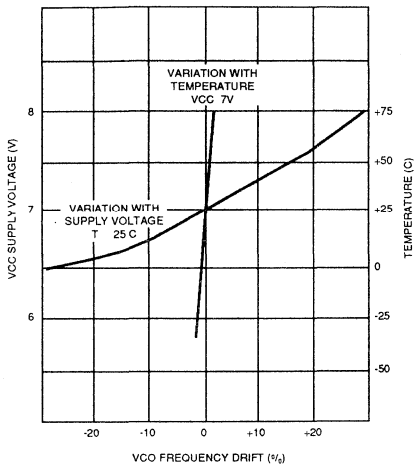


Fig. 9 Typical VCO characteristics

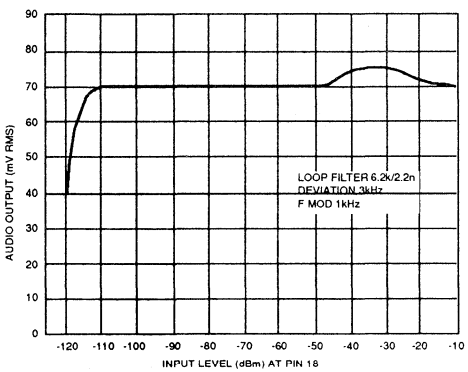


Fig. 7 Typical recovered audio v. input level (3kHz deviation)

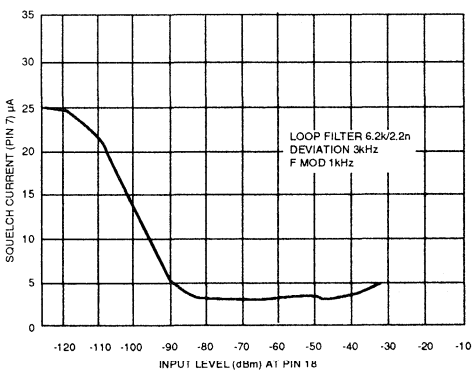


Fig. 10 Typical squelch current v. input level

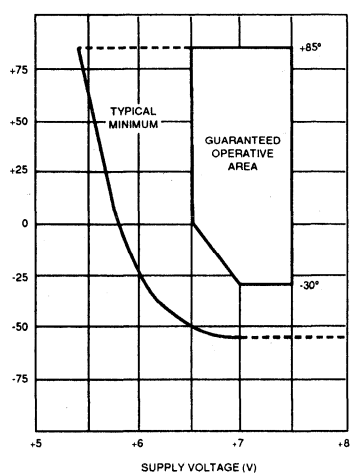


Fig. 8 Supply voltage v. temperature

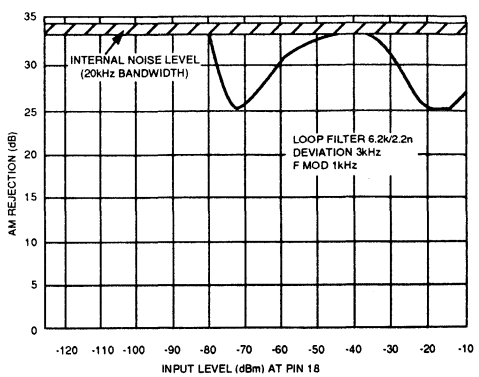


Fig. 11 Typical AM rejection

(the ratio between the audio output produced by:
(a) a 3kHz deviation 1kHz modulation FM signal and
(b) a 30% modulated 1kHz modulation AM signal at the same input voltage level.)

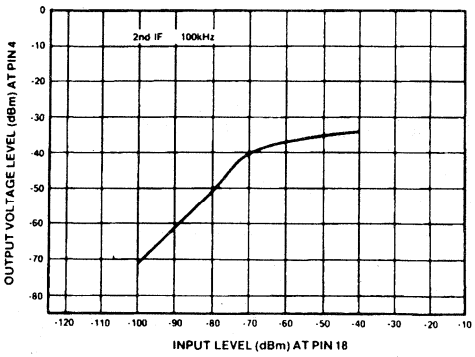


Fig. 12 Typical conversion gain (to pin 4)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	9V
Storage temperature	-55°C to +125°C (DP package)
	-55°C to +150°C (DG)
Operating temperature	-55°C to +125°C
(see Electrical Characteristics)	
Input voltage	1V RMS at pin 18

3115 2.3

SL6649-1

200MHz DIRECT CONVERSION FSK DATA RECEIVER

(Supersedes September 1991 edition)

The SL6649-1 is a low power direct conversion radio receiver for the reception of frequency shift keyed transmissions. It features the capability of 'power down' for battery conservation.

The device also includes a low battery flag indicator.

FEATURES

- Very Low Power Operation - typ. 3.7mW.
- Single Cell Operation with External Inverter
- Complete Radio Receiver in one Package.
- Operation up to 200MHz.
- 100nV Typical Sensitivity.
- Operates up to 1200 BPS.
- On Chip Tunable Active Filters.
- Minimum External Component Count
- Low Power Down Current Typical 5μA.

APPLICATIONS

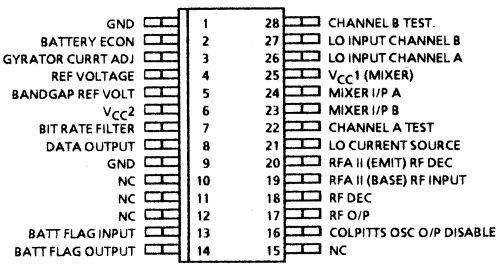
- Low Power Radio Data Receiver.
- Wristwatch Credit Card Pager.
- Radio Paging.
- Ultrasonic Direction Indication.
- Security Systems.
- Remote Control Systems

ABSOLUTE MAXIMUM RATINGS

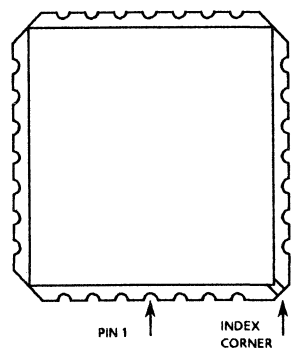
Supply Voltage	6V
Storage Temperature	-55°C to +150°C
Operating Temperature	- 20°C to +70°C

ORDERING INFORMATION

SL6649-1/CG/LCAS - Ceramic chip (LC28) carrier in tubes
SL6649-1/CG/MPES - Small outline (MP28) supplied in tubes
SL6649-1/CG/MPEF - Small outline (MP28) supplied in tape & reel
SL6649-1/CG/LCAF - Ceramic chip (LC28) carrier in tape & reel



MP28



LC28

PIN	DESCRIPTION	PIN	DESCRIPTION
1	GND	28	CHANNEL B TEST.
2	BATTERY ECON	27	LO INPUT CHANNEL B
3	GYRATOR CURRT ADJ	26	LO INPUT CHANNEL A
4	REF VOLTAGE	25	$V_{CC}1$ (MIXER)
5	BANDGAP REF VOLT	24	MIXER I/P A
6	$V_{CC}2$	23	MIXER I/P B
7	BIT RATE FILTER	22	CHANNEL A TEST
8	DATA OUTPUT	21	LO CURRENT SOURCE
9	GND	20	RFA II (EMIT) RF DEC
10	NC	19	RFA II (BASE) RF INPUT
11	NC	18	RF DEC
12	NC	17	RF O/P
13	BATT FLAG INPUT	16	COLPITTS OSC O/P DISABLE
14	BATT FLAG OUTPUT	15	NC

N.B. It is advisable to connect NC pins to ground.

Fig.1 Pin connections - Top view

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions unless otherwise stated.
$T_{amb} = 25°C$, $V_{CC}1 = 2.5V$ $V_{CC}2 = 3.5V$

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Voltage V_{CC} 1	25	V_R	1.3	2.8	V	$V_{CC}1 \leq (V_{CC}2) - 0.7$
Supply Voltage V_{CC} 2	6,16	1.8	2.3	3.5	V	
Supply Current I_{CC} 1	17, 25 26,27		1.6	2.0	mA	(I_{RF}) Included
Supply Current I_{CC} 2	6,16		0.65	0.80	mA	
Power Down I_{CC} 1	17,21,25, 26,27		5	12	µA	Batt Econ Low
Power Down I_{CC} 2	6,16		3	12	µA	Batt Econ Low
Bandgap Reference	5	1.15	1.22	1.35	V	
Voltage Reference	4	0.93	1.0	1.13	V	
RF Amplifier						
Supply Current (I_{RF})	17	460		640	µA	
Power Down	17				µA	Included in Power Down $I_{CC}1$
Mixers						
Gain to "IF Test"		32		38	dB	L.O. inputs driven in parallel with 50mV RMS @ 50MHz. IF = 2KHz
Oscillator						
Current Source	21	230	270	330	µA	
Power Down	21				µA	Included in Power Down $I_{CC}1$
Decoder						
Sensitivity				40	µVrms	Signal injected at "IF TEST" B.E.R. ≤ 1in 30 5KHz deviation @ 500 bits/sec BRF capacitor = 1nF
Output Mark Space Ratio	8	7:9		9:7		
Output Logic High	8	85			$\%V_{CC}2$	
Output Logic Low				15	$\%V_{CC}2$	
Battery Economy						
Input Logic High	2	(VCC2) -0.3			V	Powered Up
Input Logic Low	2			0.3	V	Powered Down
Input Current			0.05	1	µA	
Battery Flag						
Output High Level	14	85			$\%V_{CC}2$	Battery Low $R_L > 1M\Omega$
Output Low Level	14			15	$\%V_{CC}2$	Battery High $R_L > 1M\Omega$
Flag trig Level	13	V_R-25mV		V_R + 25mV	V	Voltage Reference (V_R) pin 4
Colpitts Oscillator						
Frequency		15		15	kHz kHz	R = 90K, pin 3 to GND R = 360K, pin 3 to GND

TYPICAL ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed by design
T_{amb} = 25°C, V_{CC} 1 = 2.5V V_{CC}2 = 3.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
RF Amplifier						
Noise Figure			5.5		dB	RS = 50Ω
Power Gain			14		dB	
Input Impedance	19					See Fig. 8
Mixer						
RF Input Impedance	23, 24					See Fig 9 (a) and (b)
LO Input Impedance	26, 27					See Fig 10
LO DC Bias Voltage	26, 27				V	Equal to pin 25.
Detector						
Output Current	7		±4		μA	
Colpitts Oscillator						
Frequency	16		15		kHz	R = 270K, Pin 3 to GND
Output Voltage	16		20		mVp-p	RL ≫ 1MΩ N.B. Refer to Channel Filter Fig. 4.

RECEIVER CHARACTERISTICS (GPS Demonstration Board)

Measurement conditions (unless otherwise stated): Applications circuit diagram Fig.6; V_{CC}1 = 1.3V; V_{CC}2 = 2.3V; T_{amb} = 25°C, ; Collpitts oscillator resistor = 270kΩ; mixer input A and B phase balance = 180°; local oscillator input A and B phase balance = 90°. Measurement methods as described by CEPT Res 2 specification. F_{IN} = 153MHz (512 baud)

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Terminal Sensitivity Tone only 4/5 call reception			-127	-124	dBm	Δf = 4.5kHz, R_S = 50Ω, Fm = 256Hz
Deviation Acceptance			±2.5		kHz	3dB De-Sensitisation. $F_{IN} = F_{LO}$
Centre Frequency Acceptance		±2.0	±2.5		kHz	Δf = 4.5kHz fm = 256Hz (512Bps)
Adjacent Channel Rejection		65	70		dB	Δ f = 4.5kHz Channel Spacing 25KHz
Adjacent + 1 Channel Regection		65	70		dB	External capacitors on test
Third Order Intermod adj-1 + adj-2		52	53		dB	pins A and B.

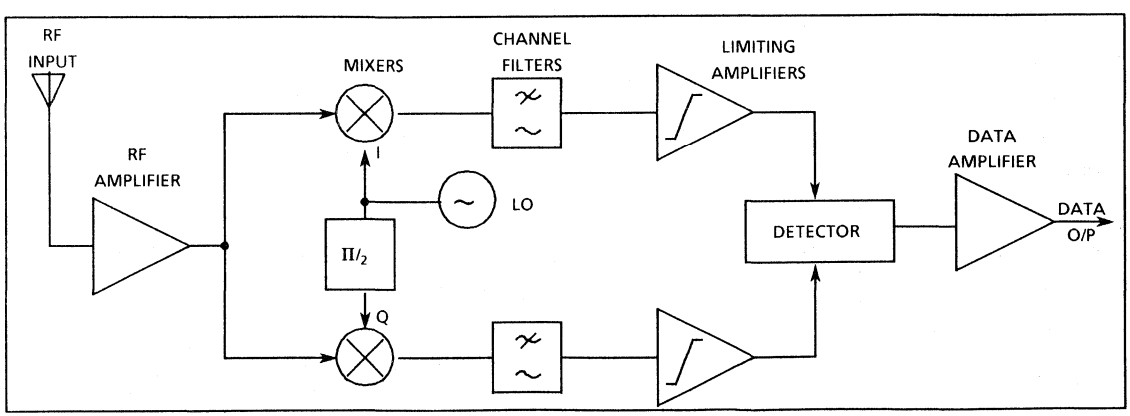


Fig.2 Block Diagram of SL6649-1 Direct Conversion Receiver

PRINCIPLE OF OPERATION

The incoming signal is split into two parts and frequency converted to baseband. The two paths are produced in phase quadrature (see Fig 2) and detected in a phase detector which provides a digital output. The quadrature network must be in the local oscillator path.

At a data rate of 512 baud and a deviation frequency of 4.5kHz, the input to the system has a demodulation index of 18. This gives a spectrum as in Fig 3. f_1 and f_0 represent the 'steady state' frequencies (i.e. modulated with continuious '1' and '0' respectively). The spectrum in Fig 3 is for reversals (a 0-1-0-1-0-1 etc. pattern) at the system bit rate; f_c is the nominal carrier frequency).

When the LO is at the nominal carrier frequency, then a continuous '0' or '1' will produce an audio frequency, at the output of the mixers corresponding to the difference between f_0 and f_c or f_1 and f_c. If the LO is precisely at f_c, then the resultant output signal will be at the same frequency regardless of the data state; nevertheless, the relative phases of the two paths will reverse between '0' and '1' states. By applying the amplified outputs of the mixers to a phase discriminator, the digital data is reproduced.

TUNING THE CHANNEL FILTERS

The adjacent channel rejection performance of the SL6649-1 receiver is determined by the channel filters. To obtain optimum adjacent channel rejection, the channel filters' cut off frequency should be set to 8KHz. The process tolerences are such that the cut off frequency can not be accurately defined, hence the channel filters must be tuned. However the receiver characteristics on page 3 can be achieved with a fixed 270kΩ resistor between pin 3 and GND.

Tuning is performed by adjusting the current in the gyrator circuits. This changes the values of the gyrator's equivalent inductance. The cut off frequency is tuned to 8KHz. To accurately define the cut off of the channel filters, a gyrator based Colpitts oscillator circuit has been included on the SL6649-1. The Colpitts oscillator and channel filters use the same type of architecture, hence there is a direct correlation between oscillator frequency and cut off frequency. By knowing the Colpitts oscillator frequency the channel filter cut off frequency can be estimated from Figure 4.

Once the channel filters have been tuned it may be necessary to disable the Colpitts oscillator. The Colpitts oscillator is disabled by connecting the Colpitts oscillator output/disable pin (pin # 16) to V_{CC} 2. This is needed since the Collpitts oscillator may impair the performance of the receiver.

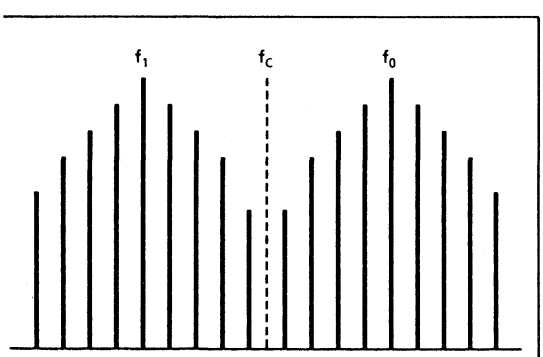


Fig. 3. Spectrum Diagram

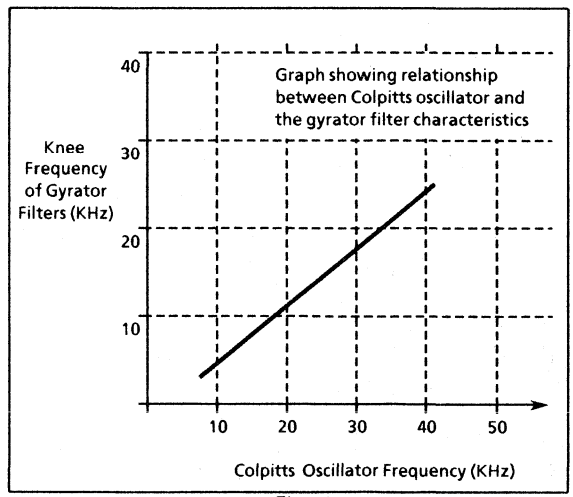


Fig. 4

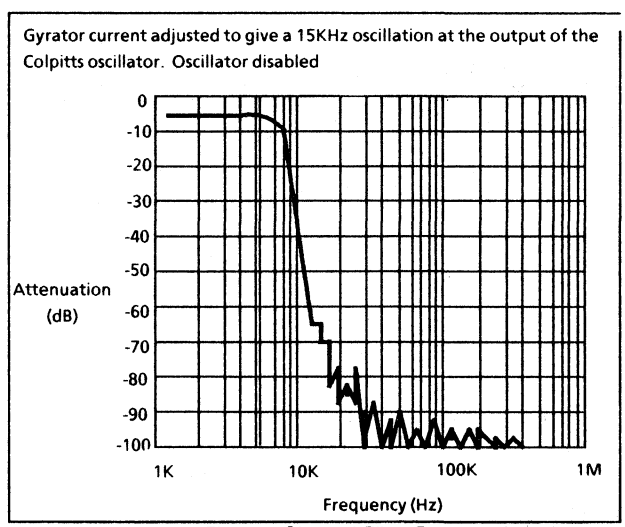


Fig. 5 Channel Filter Response

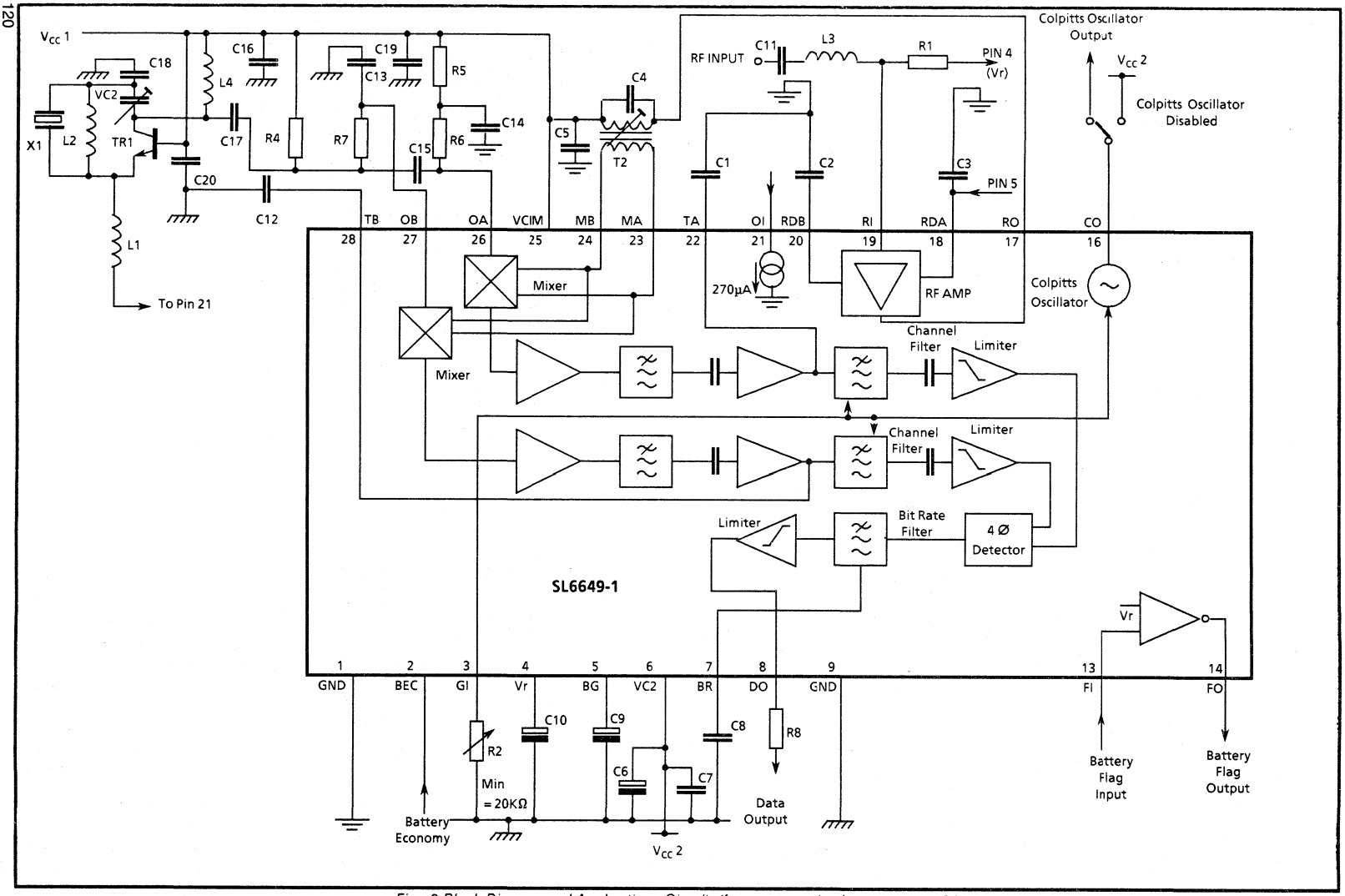


Fig. 6 Block Diagram and Applications Circuit (for component values see page 6)

COMPONENTS LIST FOR FIG.6

Capacitors	Resistors	Inductors	Transformers	Miscellaneous
C1 1nF C11 1nF C2 1nF C12 1nF C3 1nF C13 10pF C4 5.6pF C14 1nF C5 1nF C15 10pF C6 2.2µF C16 1nF C7 1nF C17 5.6pF C8 1nF C18 4.7pF C9 2.2µF C19 1nF C10 2.2µF C20 1nF	R1 2.2kΩ R2 500kΩ Variable R4 100Ω R5 100Ω R6 100Ω R7 100Ω R8 100KΩ	L1 10µH L2 220nH L3 150nH L4 100nH	T1 1:1 Transformer Primary/Secondary Inductance = 200nH	IC1 SL6649-1 TR1 SOT-23 Transistor with $f_t \geq 1.3$GHz (EG. ZETEX BFS 17) X1 153MHz 7th overtone crystal VC2 1.5-10pF

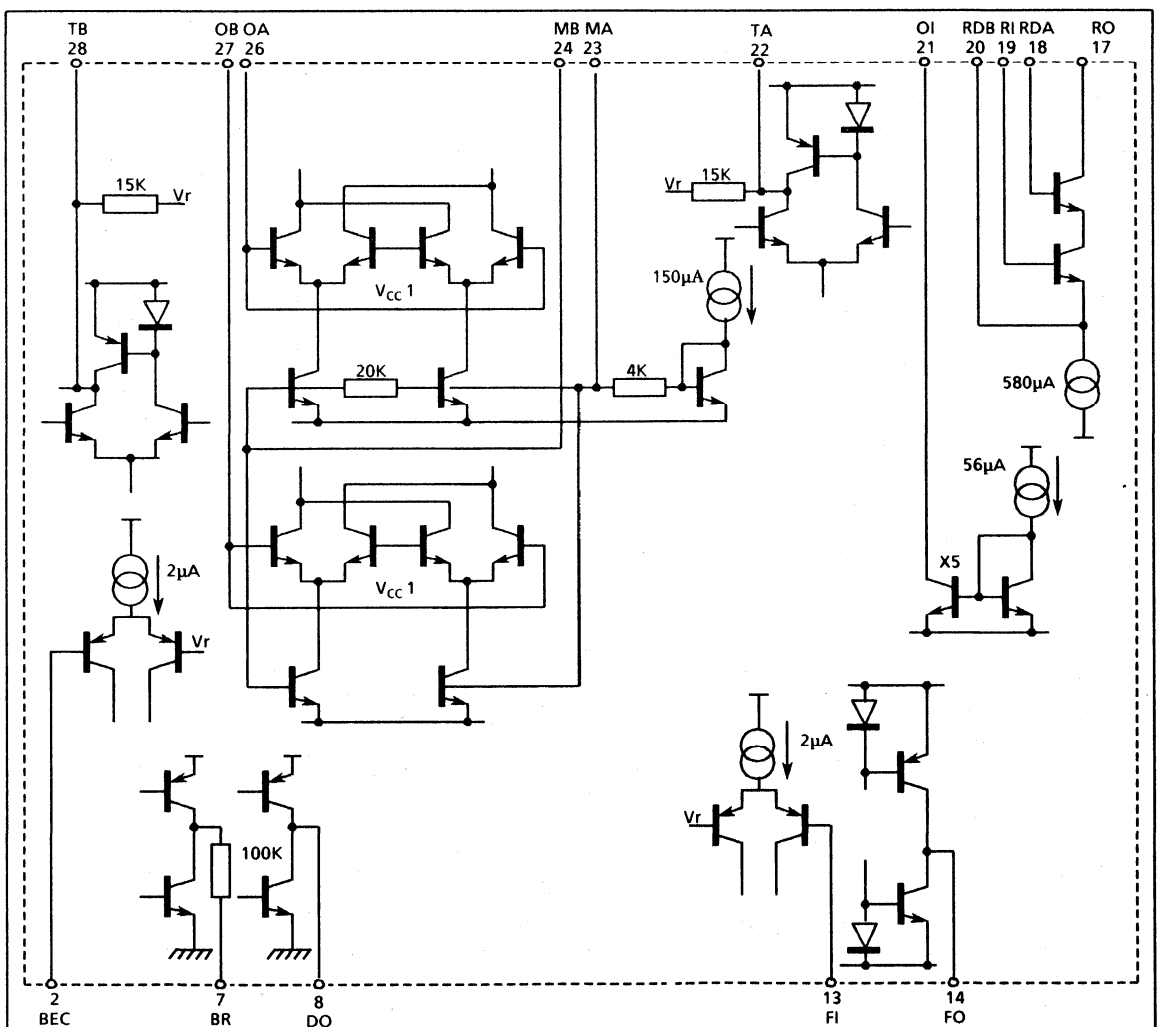
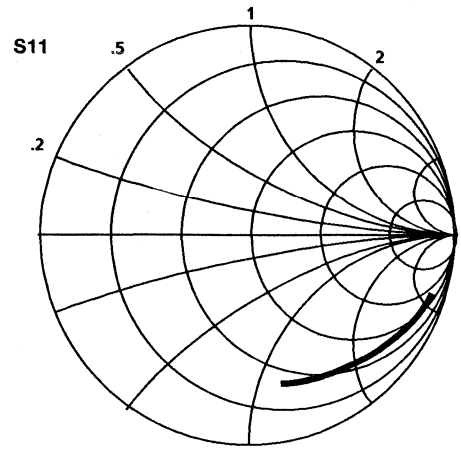
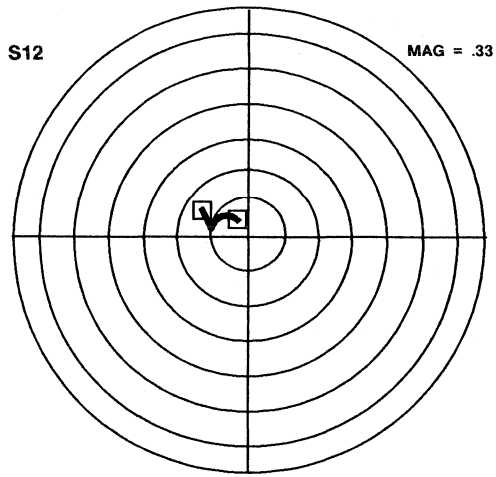
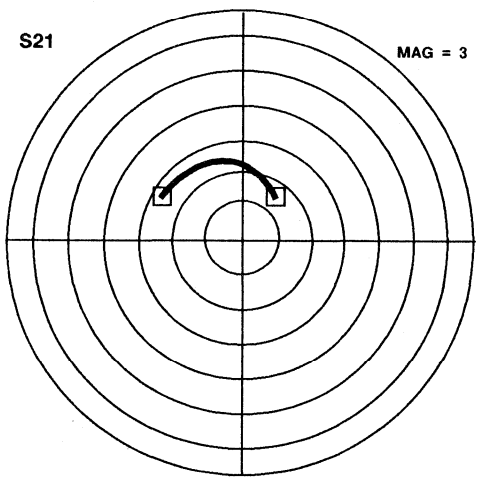
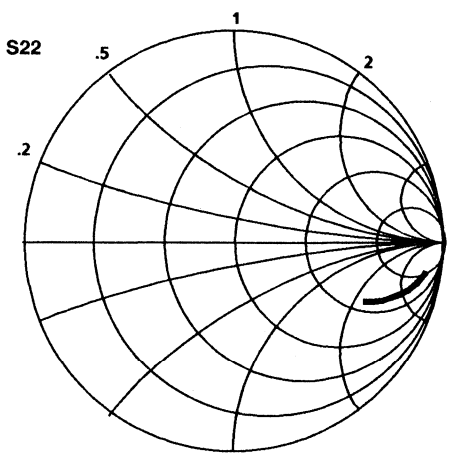


Fig. 7 Pinning Diagram of the SL6649-1









FREQ	S11		S12		S22		S21	
MHz	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.
100.000	0.963	-15.971	0.016	120.281	1.036	-3.440	1.460	157.948
150.000	0.949	-21.603	0.017	121.732	0.991	-5.524	1.390	142.732
200.000	0.934	-27.247	0.017	123.174	0.946	-7.608	1.321	127.508
250.000	0.906	-33.835	0.021	124.612	0.938	-10.156	1.261	115.531
300.000	0.876	-40.519	0.025	126.042	0.934	-12.744	1.201	103.830
350.000	0.846	-45.789	0.029	139.335	0.925	-14.380	1.132	95.446
400.000	0.816	-50.979	0.032	153.381	0.915	-15.955	1.061	87.270
450.000	0.781	-58.616	0.039	163.051	0.872	-18.015	0.986	78.111
500.000	0.746	-66.363	0.045	172.537	0.827	-20.094	0.910	68.910
550.000	0.700	-72.624	0.062	165.197	0.771	-19.691	0.854	65.157
600.000	0.655	-78.856	0.079	157.518	0.716	-19.231	0.798	61.518

Fig. 8 RF Amplifier

☐ S11

FREQ.	MAG.	ANG.
100.000	0.943	-14.921
150.000	0.929	-21.059
200.000	0.914	-27.208
250.000	0.904	-35.234
300.000	0.895	-43.439
350.000	0.866	-52.138
400.000	0.836	-60.882
450.000	0.796	-68.177
500.000	0.756	-75.417
550.000	0.726	-82.654
600.000	0.696	-89.883

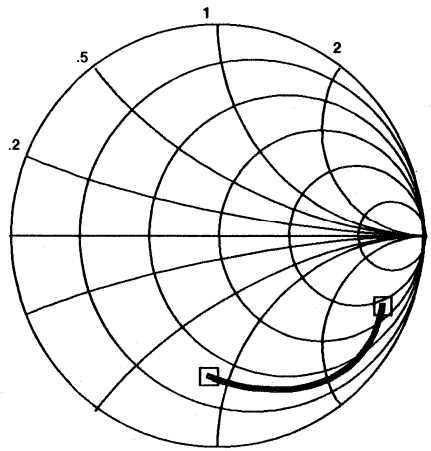


Fig. 9a SL6649-1 Mixer RF input pin. 23

☐ S11

FREQ.	MAG.	ANG.
100.000	0.963	-10.019
150.000	0.953	-15.143
200.000	0.944	-20.277
250.000	0.930	-20.764
300.000	0.915	-20.853
350.000	0.891	-30.479
400.000	0.866	-40.734
450.000	0.846	-46.135
500.000	0.826	-51.344
550.000	0.806	-57.057
600.000	0.786	-62.785

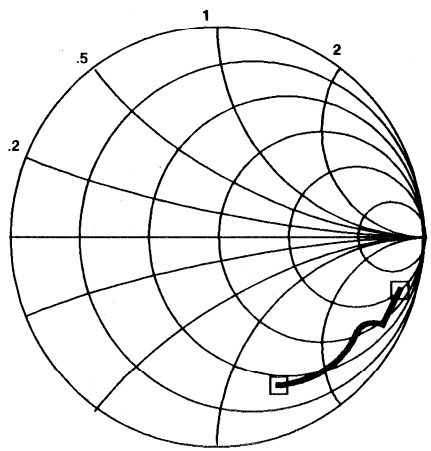


Fig. 9b SL6649-1 Mixer RF input pin. 24

☐ S11

FREQ.	MAG.	ANG.
100.000	0.993	-11.020
150.000	0.983	-16.144
200.000	0.974	-21.277
250.000	0.960	-27.820
300.000	0.945	-34.499
350.000	0.954	-39.765
400.000	0.946	-44.952
450.000	0.927	-52.586
500.000	0.907	-60.331
550.000	0.877	-67.086
600.000	0.847	-73.819

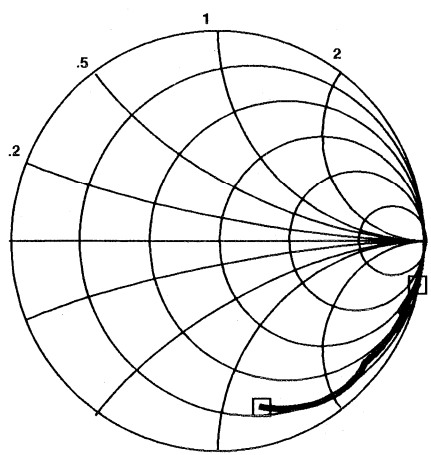


Fig. 10 SL6649-1 Mixer LO input pins 26 and 27.

METHOD FOR THE MEASUREMENT OF SENSITIVITY ON THE SL6649-1 RECEIVER

The method used by GEC Plessey Semiconductors in the measurement of terminal sensitivity is essentially the same as that described in the Cept. Res2 Specification.

This method requires the following equipment:

1. A signal generator e.g. HP8640
2. A pocsag encoder
3. A pocsag decoder e.g. MV6639
4. An SL6649-1 Demo Board.
5. An interference free low impedance P.S.U. (Vcc1 and Vcc2 must be separate supplies and there must be at least 0.7V difference between them). Recommended supply configurations are shown in Fig. 13.

The test equipment and D.U.T. are set up as shown in Fig. 11.

The R.F. frequency is set to the nominal L.O. frequency of the receiver and the peak deviation is set to 4.5KHz.

Care must be taken to avoid long power supply leads and any ground loops. Any interference from the decoder will be reduced by the insertion of a high value resistor R1 (100KΩ)between the receiver data output and the decoder input.

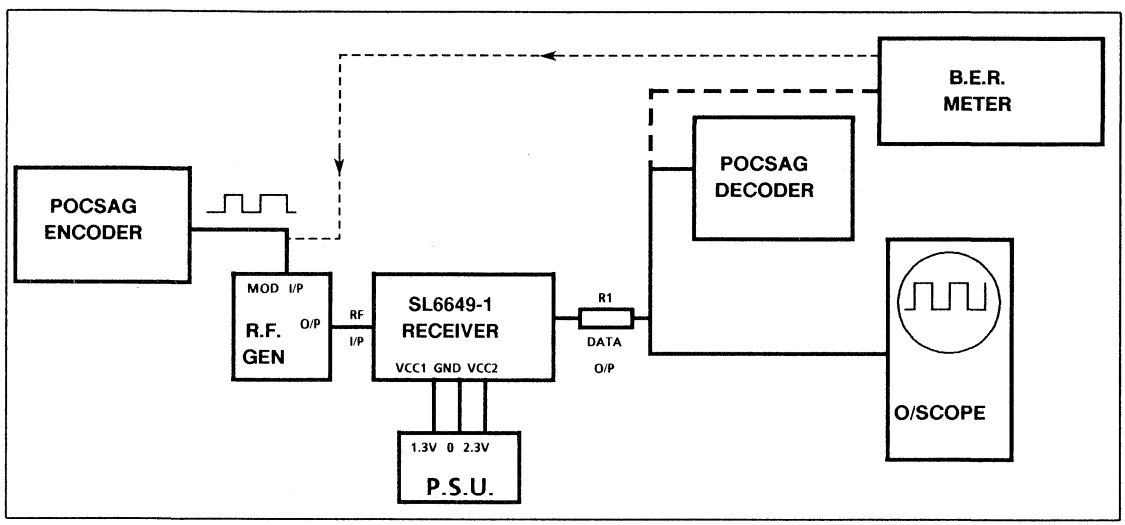


Fig. 11 Test System

The generator output level is reduced successively until the decoder responds just 4 out of 5 times to the encoder signal. This output level is then recorded as the sensitivity threshold of the receiver.

We find that this threshold correlates to a bit error rate of 1 in 30. The data output waveforms for an input level which produces a B.E.R. of 1 in 30 and for input levels 2dB above and below this level, are shown below (square wave input). It can be seen that the edge jitter increases dramatically at signal levels below the sensitivity threshold of -127dBm. Typical waveforms that can be seen on an oscilloscope around the sensitivity threshold level are shown in Fig. 12.

NB. In performing the sensitivity measurement great care should be taken in preventing coupling between test leads.

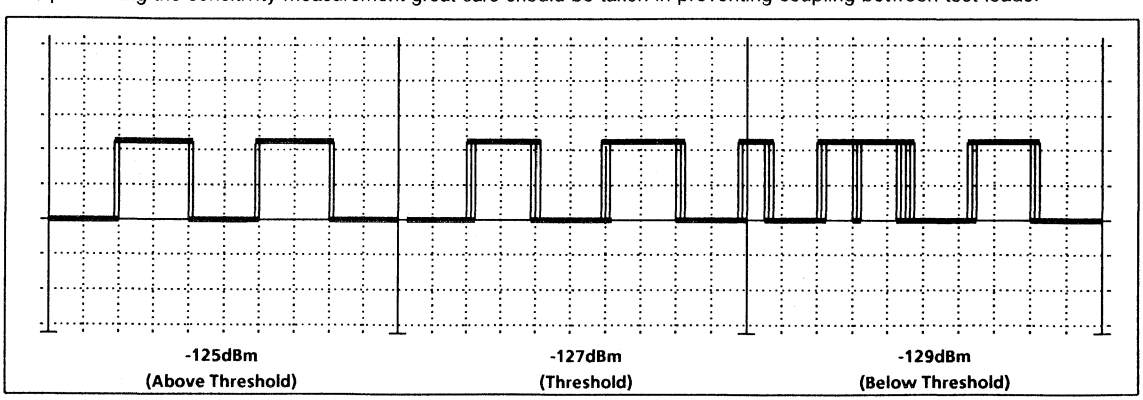
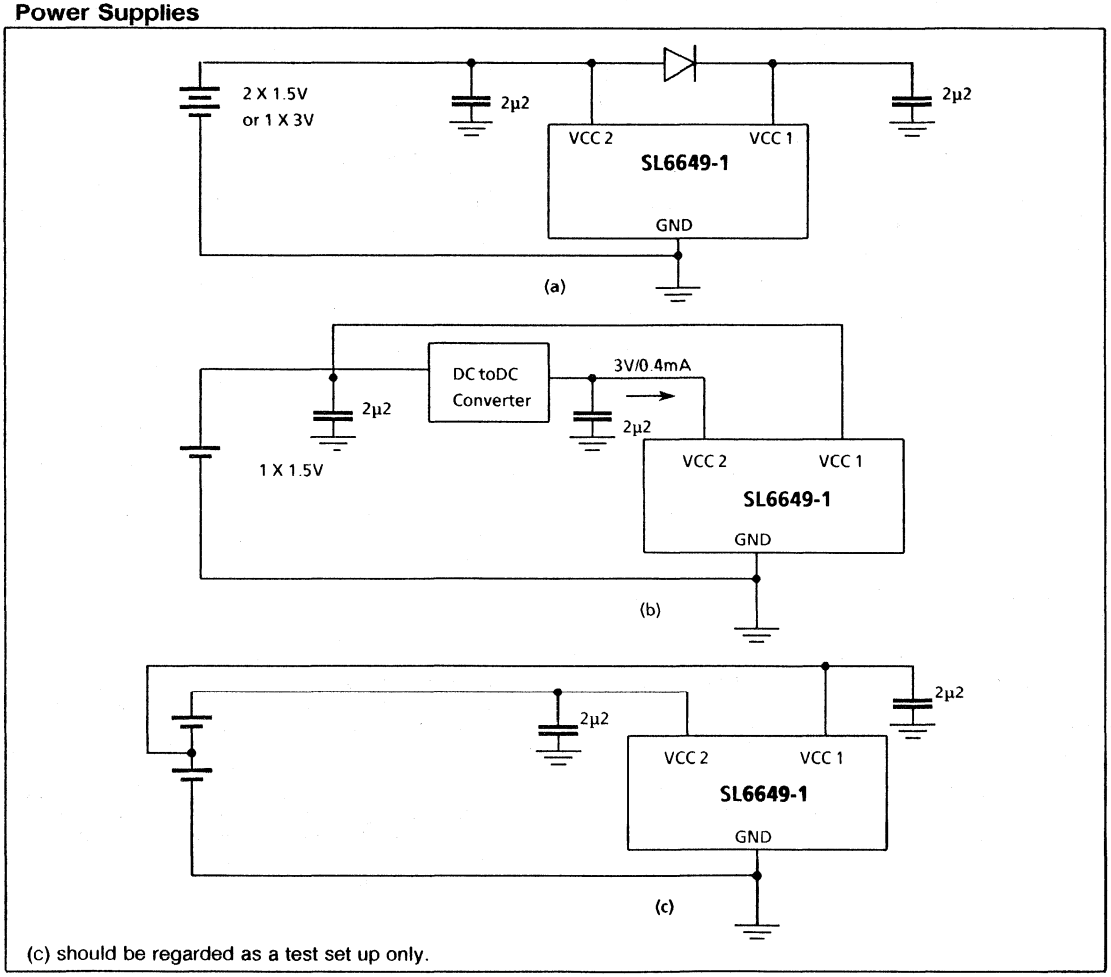


Fig. 12. Waveform at Data O/P

PIN	MNEMONIC	FUNCTION
1	GND	Ground
2	BEC	Battery Economy
3	GI	Gyrator Current Adjust
4	Vr	Reference Voltage
5	BG	Bandgap Reference Voltage
6	Vc2	V_{cc} 2
7	BR	Bit rate Filter
8	DO	Data Output
9	GND	Ground
10		UNC
11		UNC
12		UNC
13	FI	Battery Flag Input
14	FO	Battery Flag Output

PIN	MNEMONIC	FUNCTION
15		UNC
16	CO	Colpitts Oscillator Output/Disable
17	RO	RFA I (collector) RF Output
18	RDA	RFA I (base) RF Decouple
19	RI	RFA II (base) RF Input
20	RDB	RFAII (emitter) RF Decouple
21	OI	LO Current Source
22	TA	Channel A Test
23	MA	Mixer I/P B
24	MB	Mixer I/P A
25	VCIM	V_{cc}1 (mixer)
26	OA	LO Input Channel A
27	OB	LO Input Channel B
28	TB	Channel B Test

Power Supplies



(c) should be regarded as a test set up only.

Fig. 13 (a) SL6649-1 Power Supply Options

PAGER APPLICATION EXAMPLE

A typical 1 volt pager system suitable as a wrist watch application is shown in Fig. 13 (b). Only 3 integrated circuits are required to perform all the functions of a tone only pager. These are SL6649-1 direct conversion radio receiver and the MV6639 POCSAG decoder plus a 1 volt E2PROM (eg Seiko Epson SPM28C51).

The SL6649-1 receives and demodulates the data, and monitors the battery voltage. The interface between the decoder and receiver consists of only 3 connections excluding the supplies.

The MV6639 performs all the function required for a POCSAG decoder for tone only and/or pager messaging at 512 or 1200 baud. A 32KHz watch crystal is used as the reference frequency for the decoder.

The decoder voltage doubler output V_{CC2} is available to power not only the receiver, but an alternative higher voltage E²PROM and microprocessor/LCD driver for a full tone and message pager.

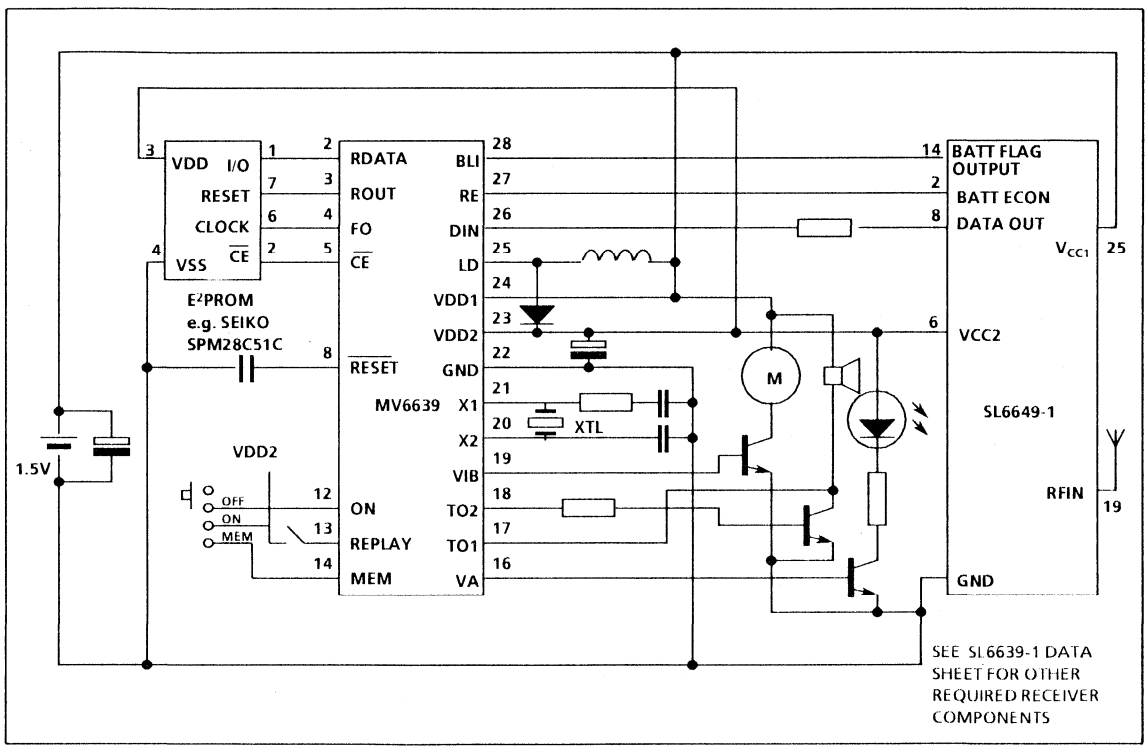


Fig. 13 (b) Toner Pager applications example showing interface with SL6649-1 receiver

OPERATION AT OTHER FREQUENCIES AND DATA RATES

The values given in the components list on page 6 are appropriate for frequencies nominally around 153MHz. In order to use the receiver at other frequencies it is necessary to change the capacitor C4 which is resonant with the transformer T1, and L2 and L4 in the oscillator circuit.

It is also necessary to change the values of capacitors C13 and C15 such that the reactance of these is equal to 100Ω at the required frequency.

It is of course necessary to use a crystal of the required frequency and stability. In order to use the receiver at higher data rates it is only necessary to reduce the value of C8, for example, at 1200bps, C8 = 470pf.

A demonstration board has been designed specifically to demonstrate terminal sensitivity. It is possible to connect an antenna to the board with suitable matching but no guarantee can be given regarding field strength sensitivity However, with a suitably designed combination of PCB and antenna, a sensitivity of 5μV/M should be attainable.

DS 3285 -1

SL6652

LOWER POWER IF/AF CIRCUIT (WITH RSSI) FOR FM CELLULAR RADIO

The SL6652 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.

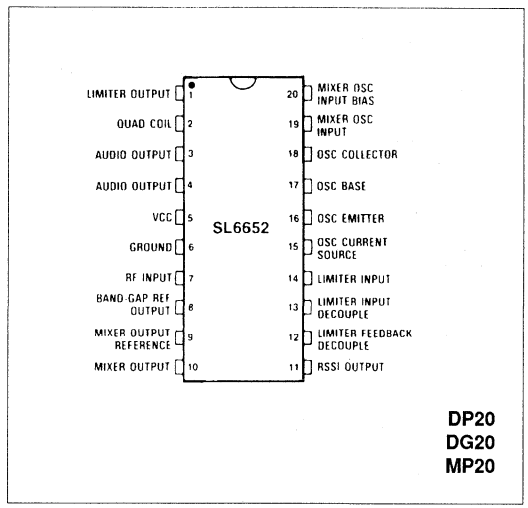


Fig. 1 Pin connections (top view)

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation
- Exceptionally Stable RSSI

APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

QUICK REFERENCE DATA

- Supply Voltage 2.5V to 7 5V
- Sensitivity 3µV
- Co-Channel Rejection 7dB

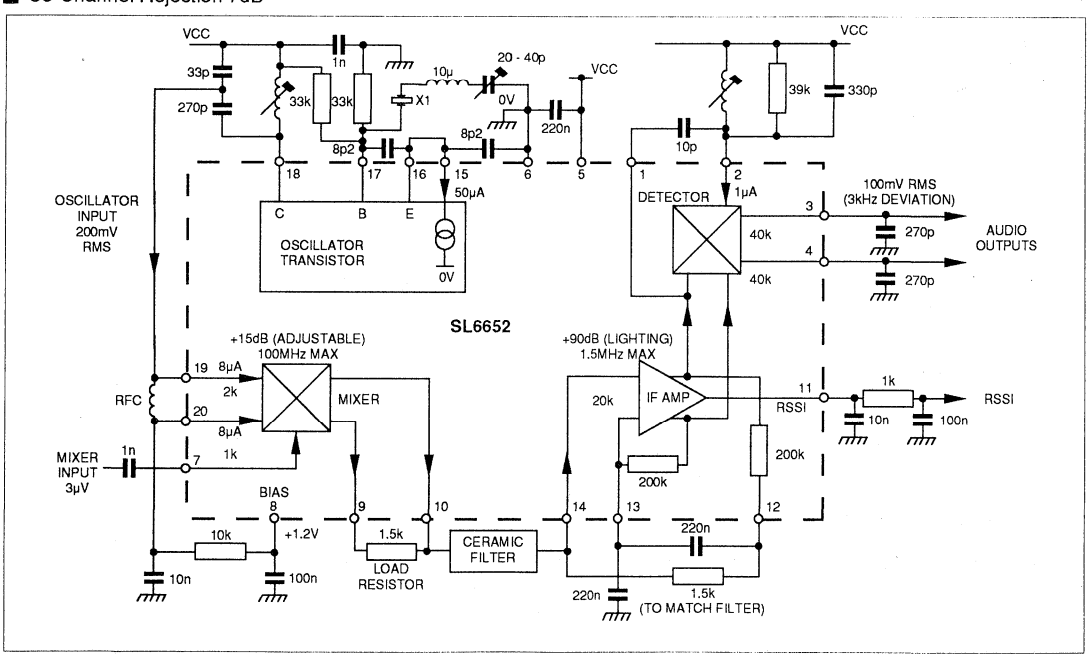


Fig. 2 block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C
Mixer input	1V rms

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{CC} = 2.5V to 7.5V, T_{amb} = -30°C to +85°C, IF = 455kHz, RF = 50MHz, Quad Coil Working Q = 30

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	µV	20dB SINAD
		3		µV	12dB SINAD
AM rejection		40		dB	RF input <500µV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25°C
Co-channel rejection		7		dB	See Note 2
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		µA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	µA	T_{amb} = 25°C
H_{fe}	30				40 ... 70µA
f_T		500		MHz	40 ... 70µA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	} 5mV into pin 14
Ultimate S/N ratio		60		dB	
THD		0.5	5	%	
Output impedance		40		kohm	
Inter-output isolation		65		dB	1kHz
RSSI Output (T_{amb} = +25°C)					
Output current			20	µA	No input pin 14
Output current	50		80	µA	Pin 14 = 2.5mV
Current change	0.9	1.22	1.5	µA/dB	See Note 1
Linear dynamic range	70			dB	See Note 1

NOTES

1. The RSSI output is 100% dynamically tested at 5V and +20° C over a 70dB range. First the input to pin 14 is set to 2.5mV and the RSSI current recorded Then for each step of 10dB from -40 to +30dB the current is measured again. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.

2. Co-channel rejection is measured by applying a 3kHz deviation, 1 kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation, 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.

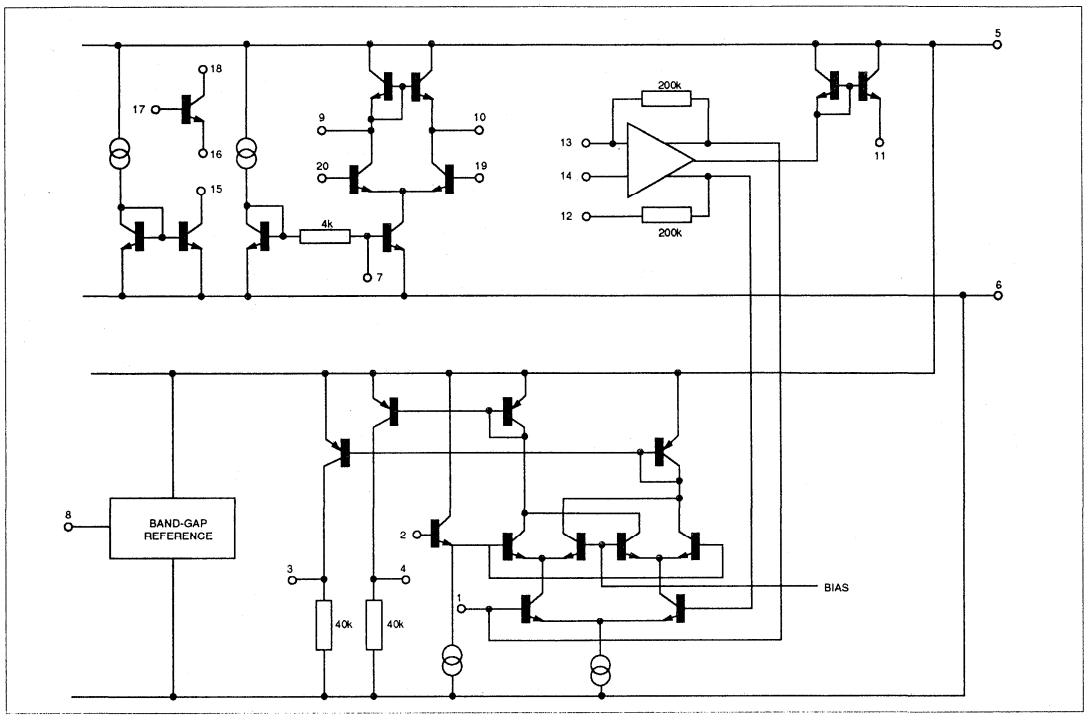


Fig. 3 Internal schematic

GENERAL DESCRIPTION

The SL6652 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to IOOMHz
- An uncommitted transistor for use as an oscillator
- A current sink for biasing this transistor
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with differential AF output
- An RSSI (Received Signal Strength Indicator) output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of an uncommitted transistor and a separate current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1 MHz and the input impedance is set by an external resistor to match the ceramic filter. Because of the high gain, pins 12 and 13 must be adequately bypassed.

Detector

A conventional quadrature detector is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network. A differential output is provided to feed a comparator for digital use, although it can also be used to provide AFC.

RSSI output

The RSSI output is a current source with value proportional to the logarithm of the IF input signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.

Supply voltage

The SL6652 will operate reliably from 2.5V to 7.5V The supply line must be decoupled with 470nF using short leads.

Detector

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is tyically 14 ohms.

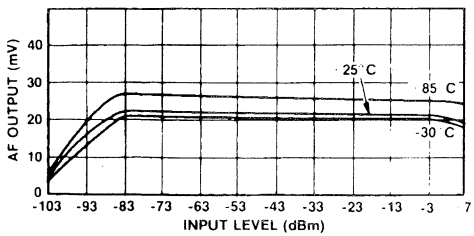


Fig. 4 Audio output vs input and temperature at 2.5V

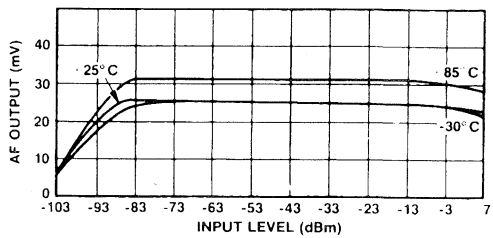


Fig. 5 Audio output vs input and temperature at 5.0V

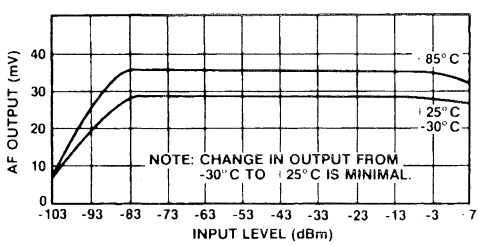


Fig. 6 Audio output vs input and temperature at +7.5V

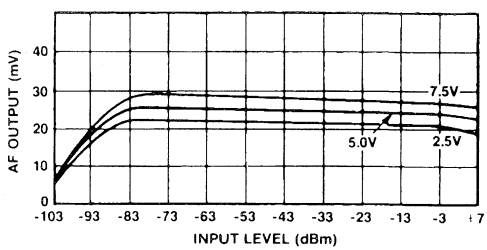


Fig. 7 Audio output vs input and supply voltage at +25°C

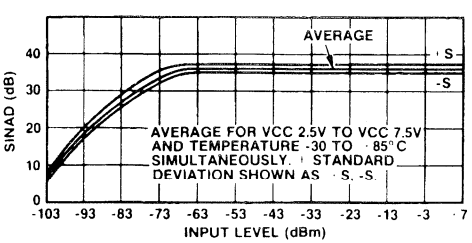


Fig. 8 SINAD and input level

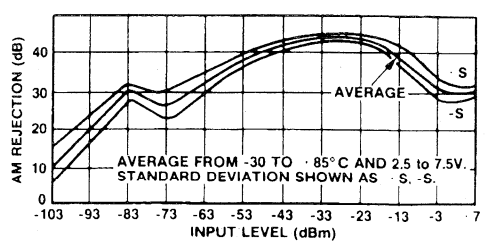


Fig. 9 AM rejection and input level

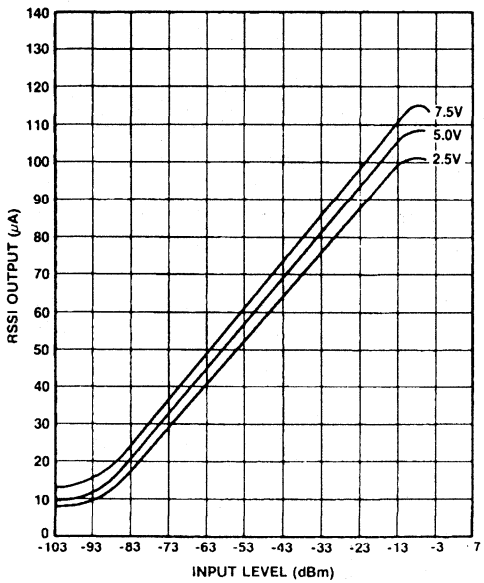


Fig. 10 RSSI output vs input and supply voltage (T_{amb} = 20°C)

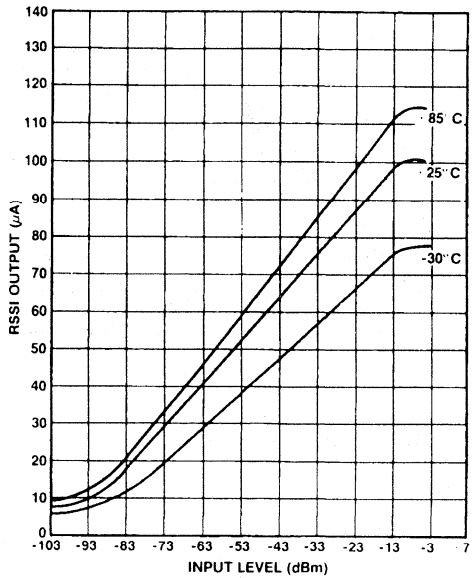


Fig. 11 RSSI output vs input level and temperature (V_{CC} = 2.5V)

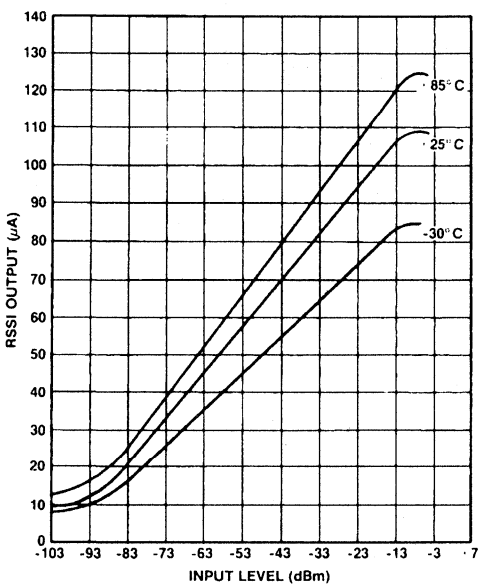


Fig. 12 RSSI output vs input level and temperature (T_{CC} = 5V)

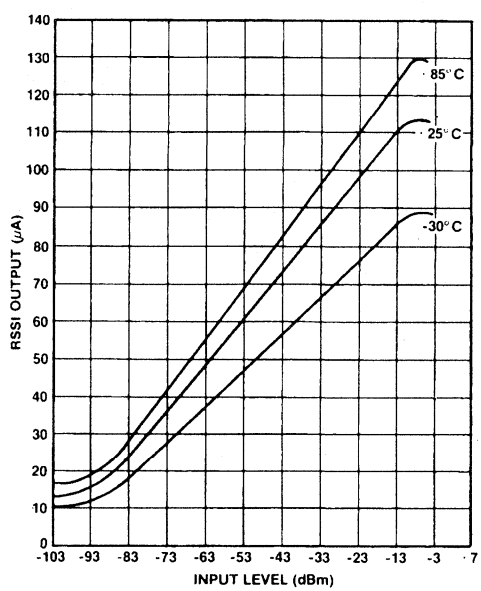


Fig. 13 RSSI output vs input level and temperature (V_{CC} = 7.5V)

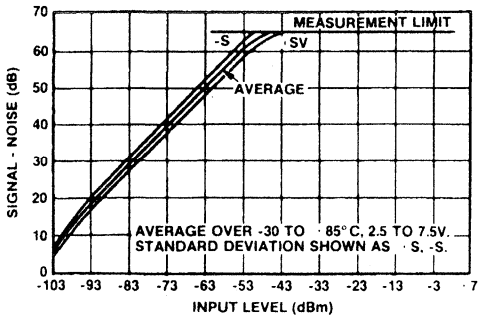


Fig. 14 Signal + noise to noise ratio vs input level

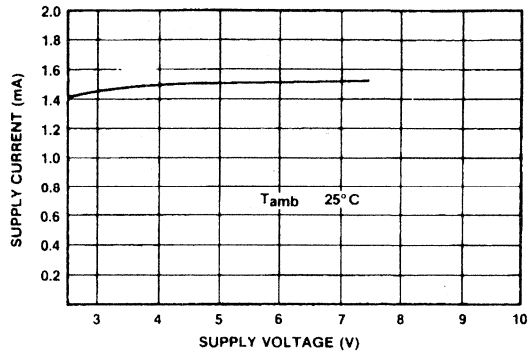


Fig. 15 Supply current vs supply voltage

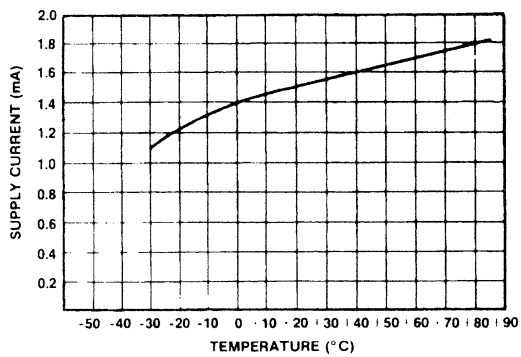


Fig. 16 Supply current vs temperature (V_{CC} = 5V)

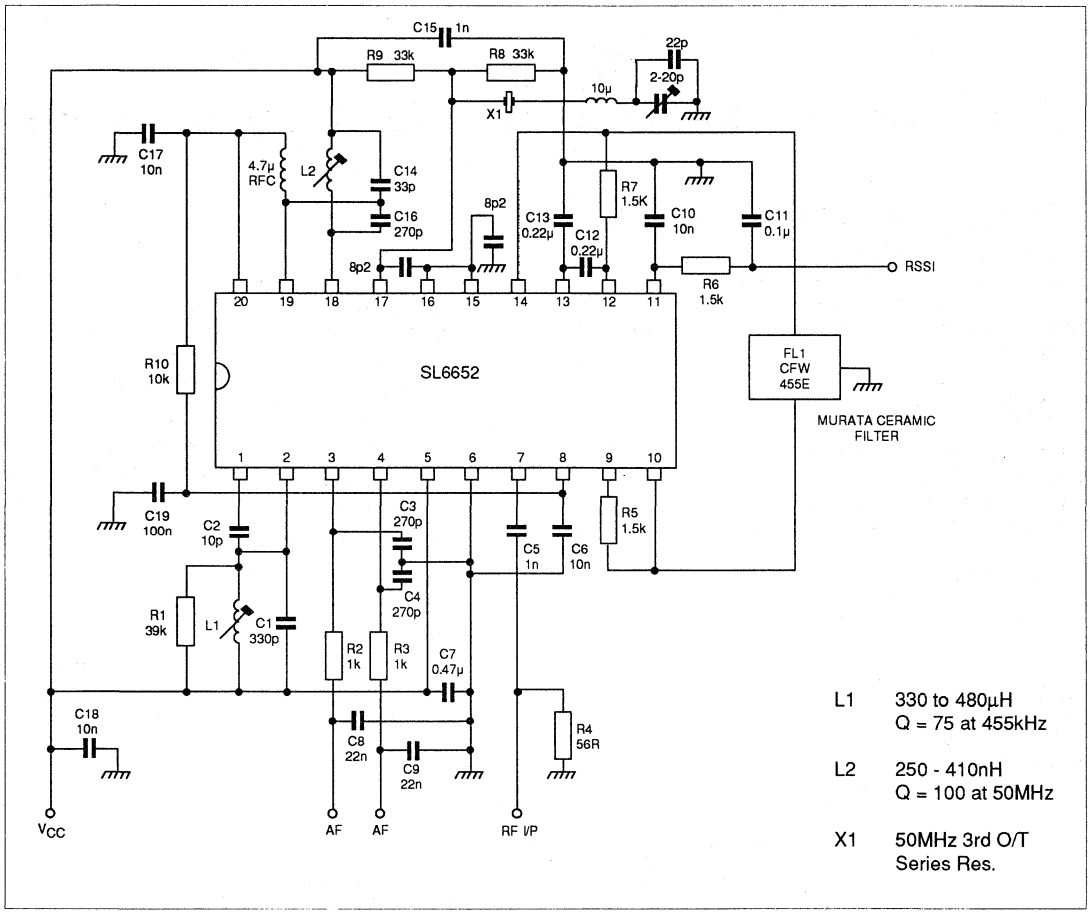


Fig. 17 Circuit diagram of SL6652 application circuit

DS 3286 -1

SL6654

LOWER POWER IF/AF CIRCUIT (WITH RSSI) FOR FM CELLULAR RADIO

The SL6654 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.

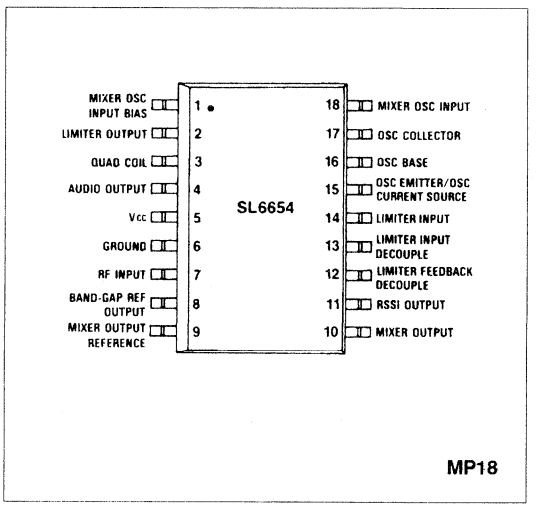


Fig. 1 Pin connections (top view)

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation
- Exceptionally Stable RSSI

APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

QUICK REFERENCE DATA

- Supply Voltage 2.5V to 7 5V
- Sensitivity 3µV
- Co-Channel Rejection 7dB

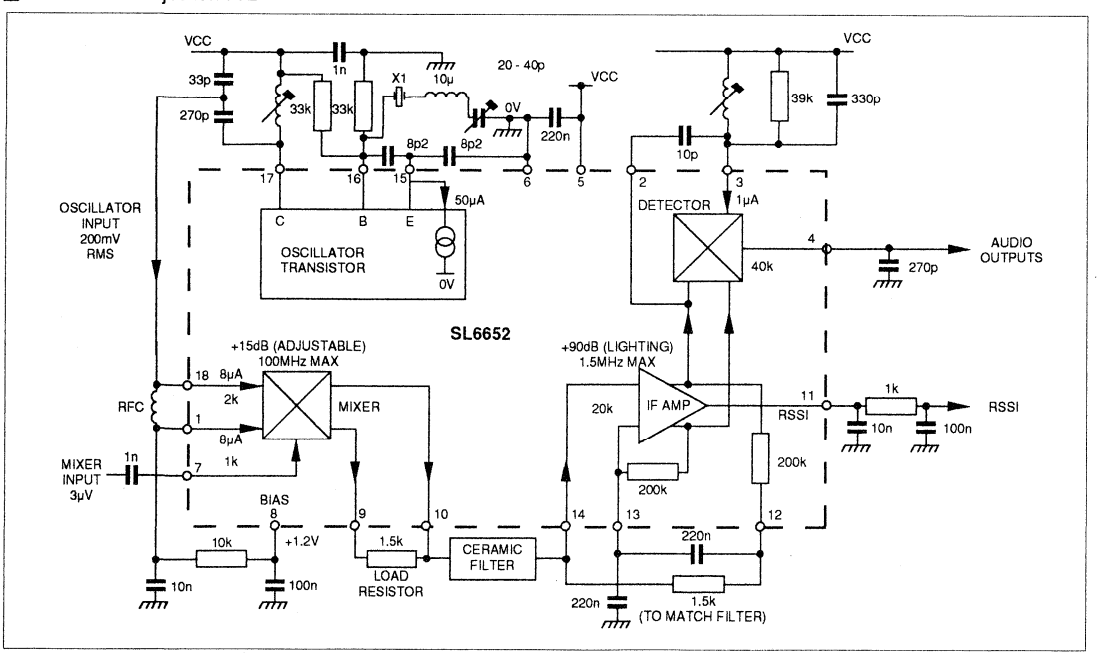


Fig. 2 block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C
Mixer input	1V rms

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{CC} = 2.5V to 7.5V, T_{amb} = -30°C to +85°C, IF = 455kHz, RF = 50MHz, Quad Coil Working Q = 30

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	µV	20dB SINAD
		3		µV	12dB SINAD
AM rejection		40		dB	RF input <500µV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25°C
Co-channel rejection		7		dB	See Note 2
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		µA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	µA	T_{amb} = 25°C
H_{fe}	30				40 ... 70µA
f_T		500		MHz	40 ... 70µA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	} 5mV into pin 14
Ultimate S/N ratio		60		dB	
THD		0.5	5	%	
Output impedance		40		kohm	
Inter-output isolation		65		dB	1kHz
RSSI Output (T_{amb} = +25°C)					
Output current			20	µA	No input pin 14
Output current	50		80	µA	Pin 14 = 2.5mV
Current change	0.9	1.22	1.5	µA/dB	See Note 1
Linear dynamic range	70			dB	See Note 1

NOTES

1. The RSSI output is 100% dynamically tested at 5V and +20° C over a 70dB range. First the input to pin 14 is set to 2.5mV and the RSSI current recorded Then for each step of 10dB from -40 to +30dB the current is measured again. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.

2. Co-channel rejection is measured by applying a 3kHz deviation, 1 kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation, 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.

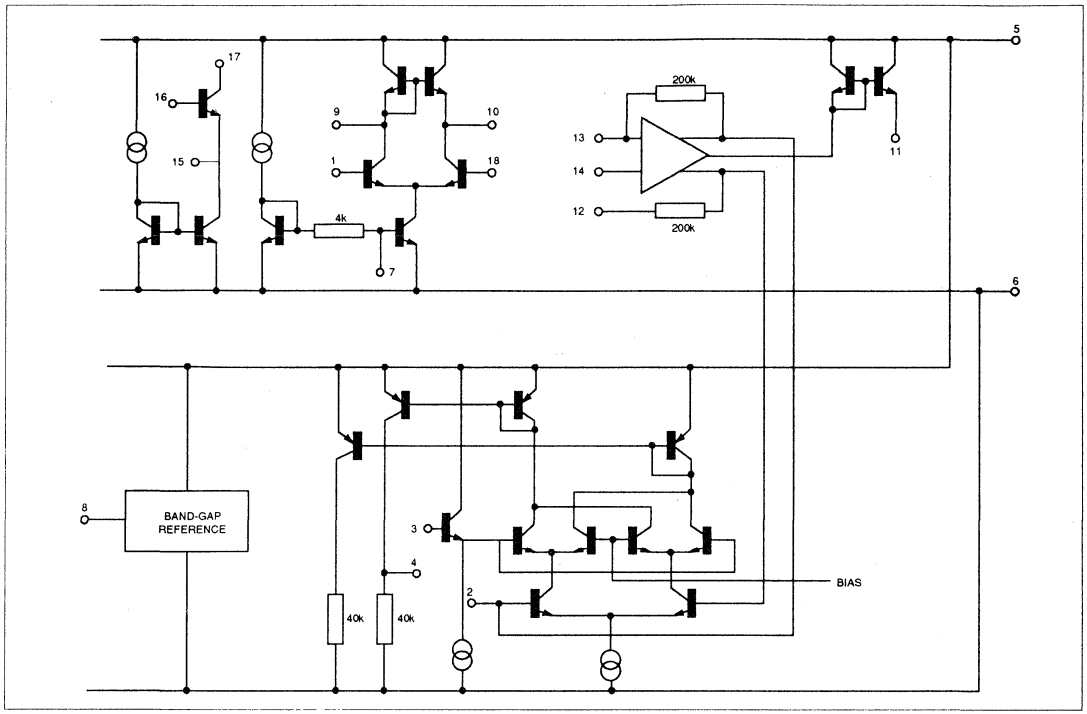


Fig. 3 Internal schematic

GENERAL DESCRIPTION

The SL6654 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to IOOMHz
- An uncommitted transistor for use as an oscillator
- A current sink for biasing this transistor
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with differential AF output
- An RSSI (Received Signal Strength Indicator) output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of an uncommitted transistor and a separate current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1 MHz and the input impedance is set by an external resistor to match the ceramic filter. Because of the high gain, pins 12 and 13 must be adequately bypassed.

Detector

A conventional quadrature detector is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network. A differential output is provided to feed a comparator for digital use, although it can also be used to provide AFC.

RSSI output

The RSSI output is a current source with value proportional to the logarithm of the IF input signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.

Supply voltage

The SL6652 will operate reliably from 2.5V to 7.5V The supply line must be decoupled with 470nF using short leads.

Detector

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is tyically 14 ohms.

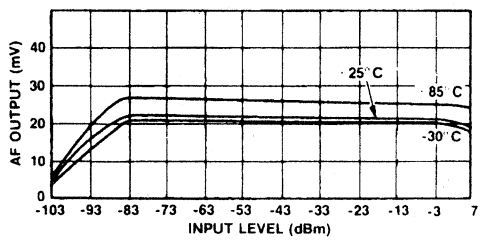


Fig. 4 Audio output vs input and temperature at 2.5V

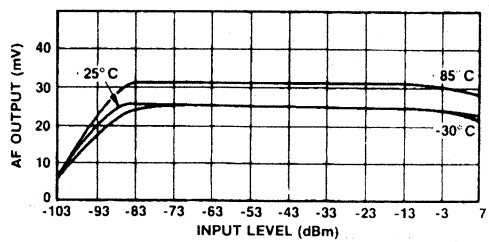


Fig. 5 Audio output vs input and temperature at 5.0V

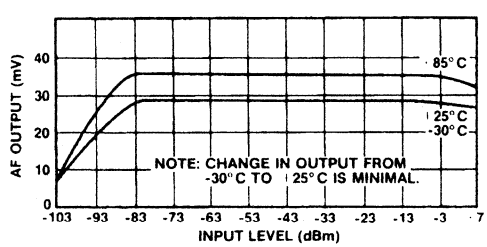


Fig. 6 Audio output vs input and temperature at +7.5V

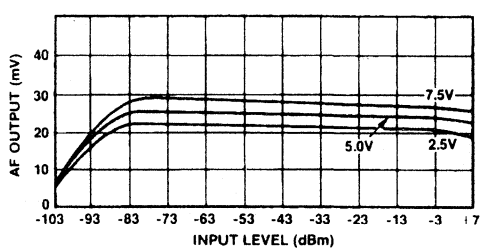


Fig. 7 Audio output vs input and supply voltage at +25°C

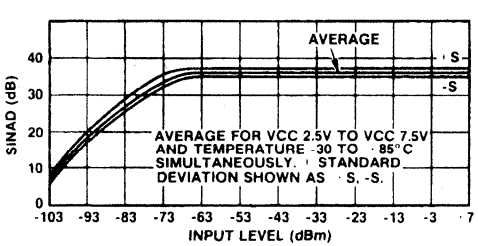


Fig. 8 SINAD and input level

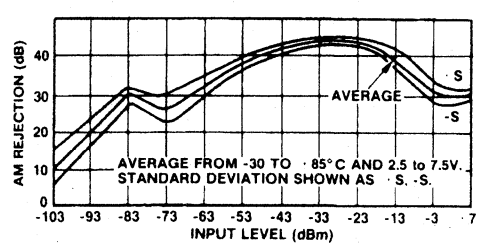


Fig. 9 AM rejection and input level

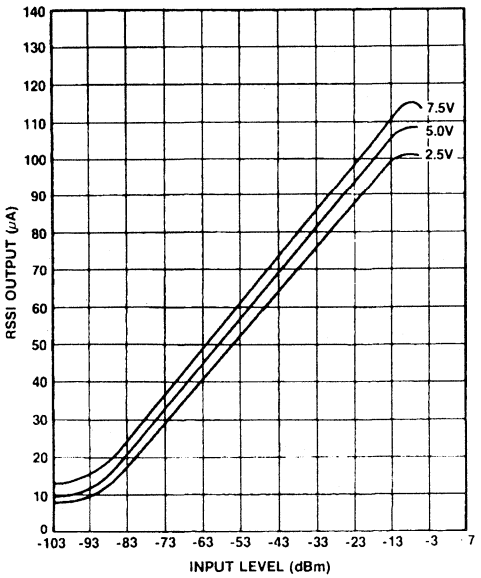


Fig. 10 RSSI output vs input and supply voltage (T_{amb} = 20°C)

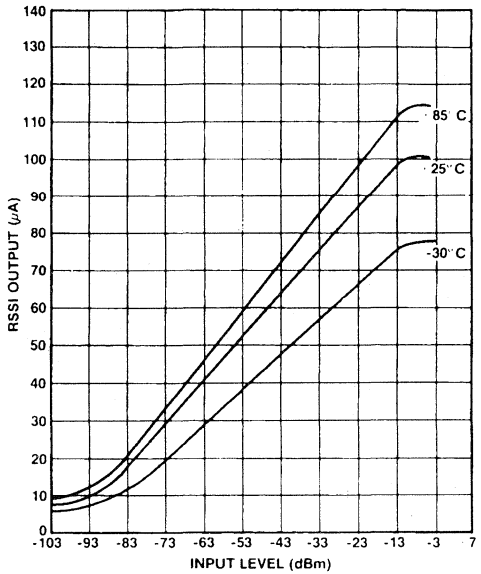


Fig. 11 RSSI output vs input level and temperature (V_{CC} = 2.5V)

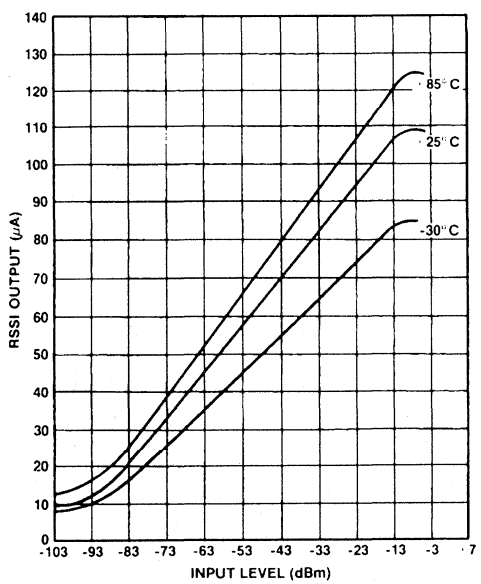


Fig. 12 RSSI output vs input level and temperature (T_{CC} = 5V)

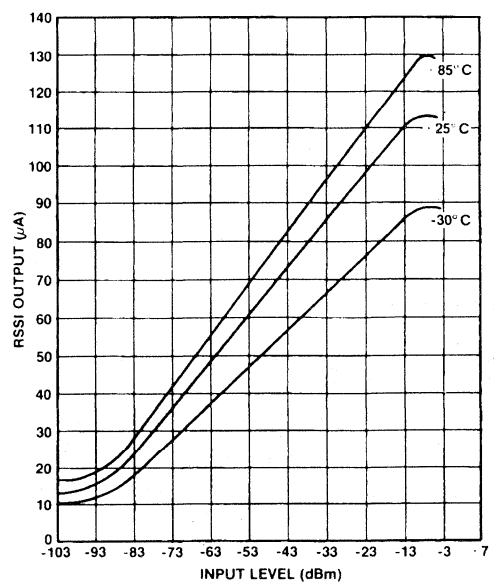


Fig. 13 RSSI output vs input level and temperature (V_{CC} = 7.5V)

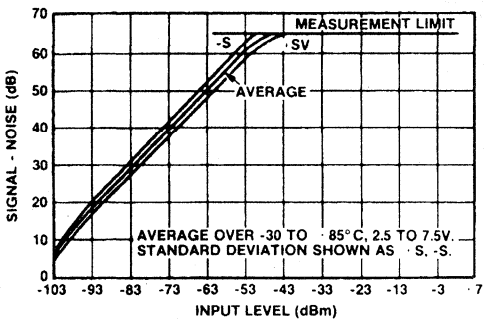


Fig. 14 Signal + noise to noise ratio vs input level

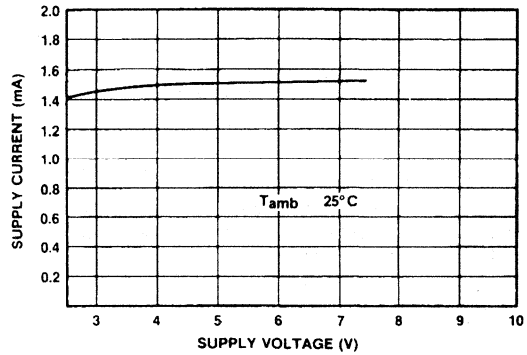


Fig. 15 Supply current vs supply voltage

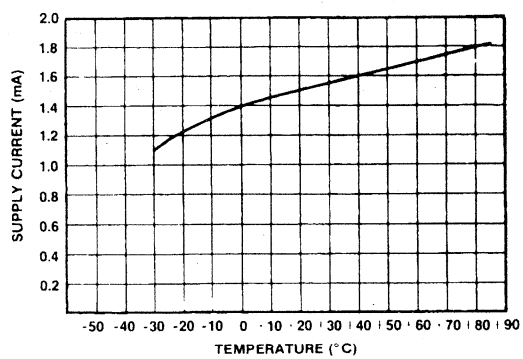


Fig. 16 Supply current vs temperature (V_{CC} = 5V)

DS 3287 -1

SL6655

ULTRA LOW POWER FM RADIO RECEIVER

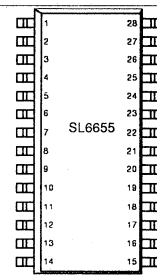
The SL6655 is a single conversion receiver complete with RF amplifier/mixer/oscillator/IF amplifier and detector. It features very low power consumption and operation from 0.95V to 5V supply The device can be powered-down to currents of 1μA and offers sensitivities of typically 250nV.

FEATURES

- Very Low Voltage Operation (0.95V)
- Very Low Current Consumption:
  1mA Powered-up (typ.)
  1μA Powered-down (typ.)
- Wide Supply Range: 0.95V to 5V
- 250nV Sensitivity (12dB Sinad)
- Guaranteed 100MHz Operation
- Miniature Plastic Surface Mount Package

APPLICATIONS

- Low Power Radio Receivers
- Radio Paging
- Cordless Telephones



Pin	Function	Pin	Function
1	N/C	15	RF Vcc +
2	Mixer output	16	LF Vcc +
3	Battery economy	17	Audio output
4	Oscillator current source & emitter	18	Audio outp-It(Differential)
5	Oscillator base	19	Quad coil drive
6	Oscillator collector	20	Quad coil
7	Mixer osc input	21	N/C
8	Mixer osc I/P bias	22	2nd limiter F/B dr couple
9	Mixer RF input	23	2nd limiter input
10	RF amp output	24	2nd limiter I/P decouple
11	Regulator output	25	1st limiter output
12	RF amp input	26	1st limiter I/P decouple
13	RF ground	27	1st limiter input
14	LF ground	28	1st limiter F/B decouple

Fig. 1 Pin connections - top view

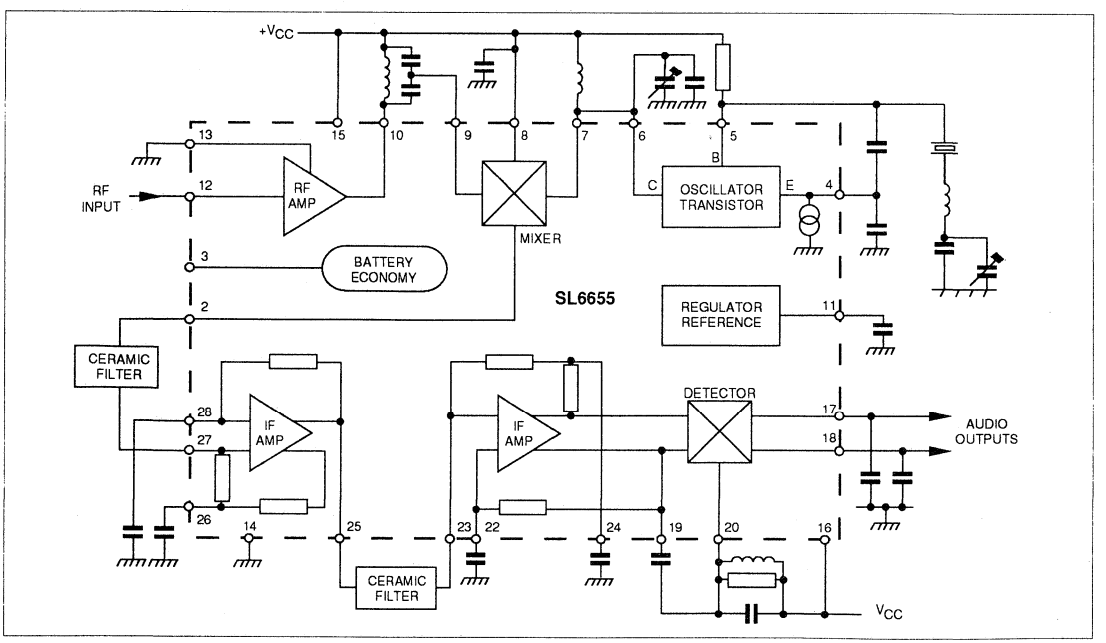


Fig. 2 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Input signal = 50MHz, Frequency modulated with 1kHz with ± 3kHz deviation, Tamb = 0°C to +50°C, Vcc = 1.3V

Characteristics	Pin Number	Value			Units	Conditions
		Min.	Typ.	Max.		
Overall						
Supply voltage		0.95		5.0	V	25°C
Supply voltage		1.05		5.0	V	-30°C to +85°C
Supply current						
Powered up			1.0	1.3	mA	Pin 3 High
Powered down			1.0		µA	Pin 3 Low
Battery economy response			0.5		ms	
Sensitivity			250		nV	12dB Sinad
AM rejection			37		dB	
RF amplifier						
Supply current			50		µA	
Noise figure			6		dB	
HFE			100			
fT			500		MHz	
Oscillator						
Supply current			50		µA	
H_{fe}			100			
f_T			500		MHz	
IF amplifier cascade						
Sensitivity	27		3		µA	12dB Sinad
Input impedance	27, 23		1.5		kΩ	
Output impedance	25		1.5		kΩ	
Gain			100		dB	
Upper cut-off frequency			1.5		MHz	
Detector						
Audio output level			12		mV(rms)	Open circuit (Quad Coil Q = 30)
Inter-output isolation			65		dB	
Output impedance			50		kΩ	
Mixer						
Conversion gain			6		dB	
Input impedance			4		kΩ	
Output impedance			1.5		kΩ	
Regulator						
Output level		0.9	0.95	1	V	
Output temperature coefficent			1.3		mV/°C	
Output current		6			mA	
Battery economy						
Input current			0.5		µA	
Input logic high		80			%/Vcc	
Input logic low				20	%/Vcc	

GENERAL DESCRIPTION

The RF amplifier is a diode biased input with a bias current of typically 50µA. The output is left open circuit so that the gain can be selected externally

The RF input to the Mixer is diode biased with a bias current of typically 250µA. The oscillator input is differential, but would normally be driven single ended with the remaining input biased at Vcc.

The Mixer has a single output with resistance of 1.5kΩ A single transistor is used for the oscillator which has its base and collector floating, and the emitter connected to a current source of 50µA nominal value.

The IF amplifiers have input impedances of 1.5kΩ and are thus ideally suited for use with 455kHz ceramic filters.

The detector is fed internally from the IF limiting amplifier and the quadrature input is fed externally using a capacitor and appropriate phase shift networks. A differential audio output is provided to feed a comparator for digital use. The regulated output is a supply independent and partially temperature compensated capable of sourcing 6mA.

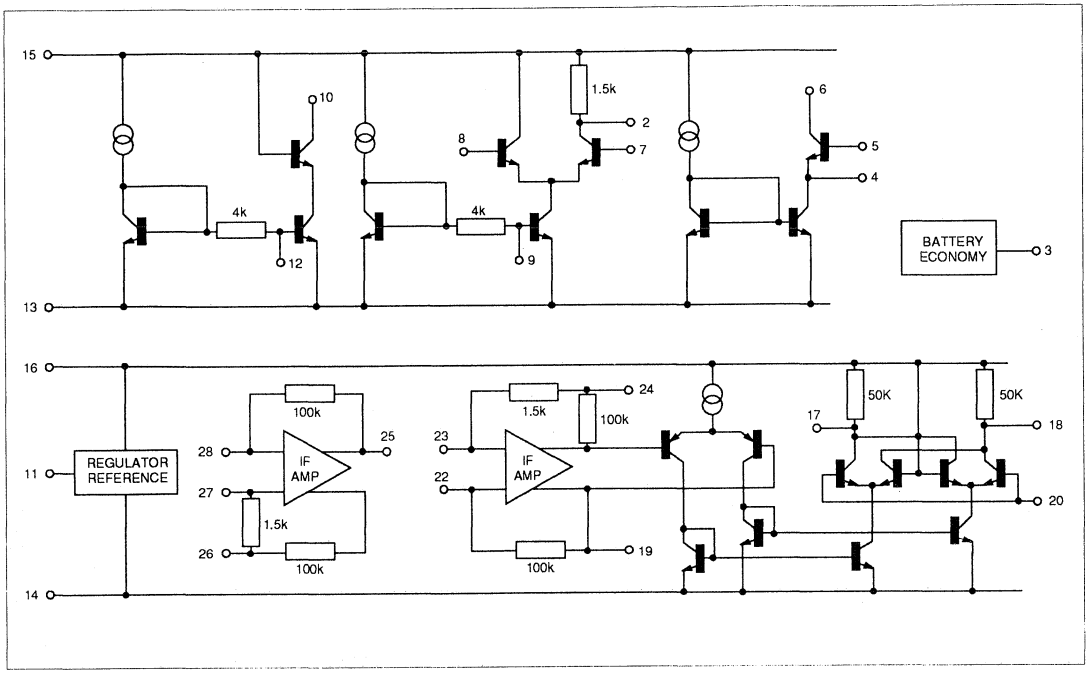
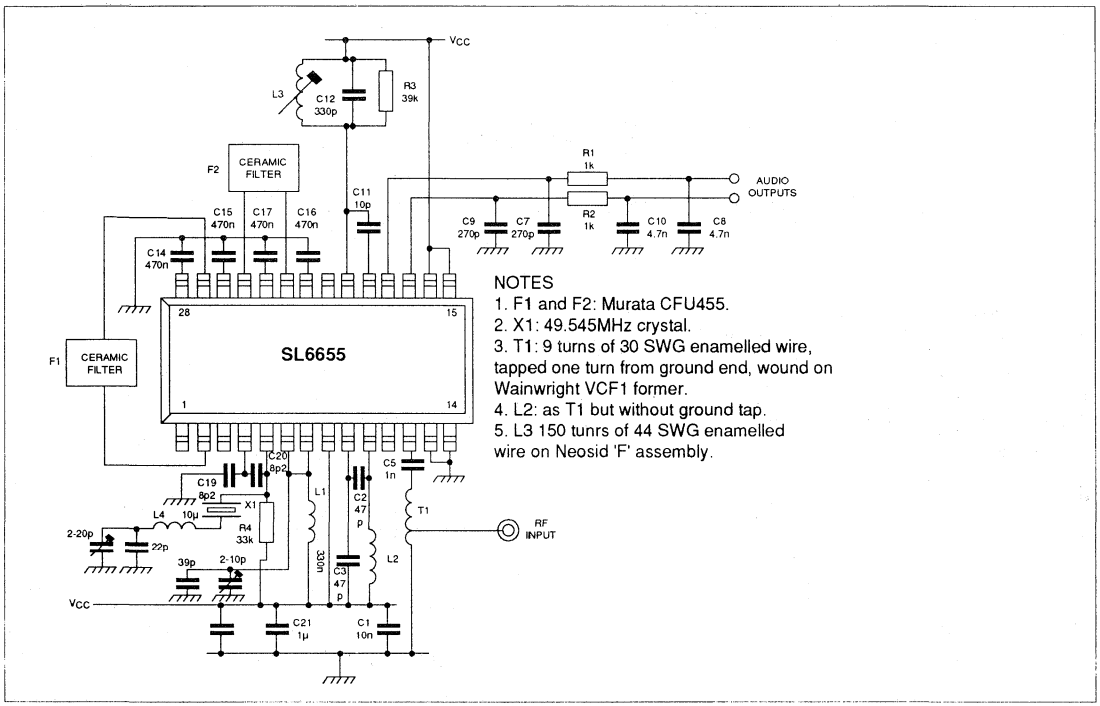


Fig. 3 SL6655 internal schematic



NOTES
1. F1 and F2: Murata CFU455.
2. X1: 49.545MHz crystal.
3. T1: 9 turns of 30 SWG enamelled wire, tapped one turn from ground end, wound on Wainwright VCF1 former.
4. L2: as T1 but without ground tap.
5. L3 150 tunrs of 44 SWG enamelled wire on Neosid 'F' assembly.

Fig. 4 Circuit diagram of SL6655 Application Circuit

PERFORMANCE OF SL6655 DEMONSTRATION BOARD

Input signal = 50MHz, Frequency modulated with 1kHz with ± 3kHz deviation, Tamb = 0°C to +50°C, Vcc = 1.3V

Sensitivity	-119dBm for 12dB sinad at 1 3V -113dBm for 12dB sinad at 0.95V
Adjacent channel rejection	50dB at 1 3V 68dB at 0.95V
Co-channel rejection	10dB at 1.3V 9dB at 0 95V
RF amplifier 2nd order intercept **RF amplifier 3rd order intercept**	0dB -14dBm
Noise figure of RF amplifier	6dB

SL6659

LOW POWER IF/AF CIRCUIT (WITH RSSI) FOR FM RADIO

The SL6659 is a complete single chip mixer, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 200MHz Operation
- Exceptionally Stable RSSI

APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

ORDERING INFORMATION

SL6659 NA MP - Miniature DIL plastic package

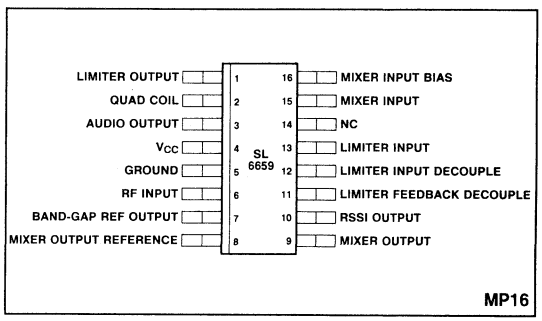


Fig.1 Pin connections (top view)

QUICK REFERENCE DATA

- Supply Voltage 2.5V to 7.5V
- Sensitivity 3μV
- Co-Channel Rejection 7dB

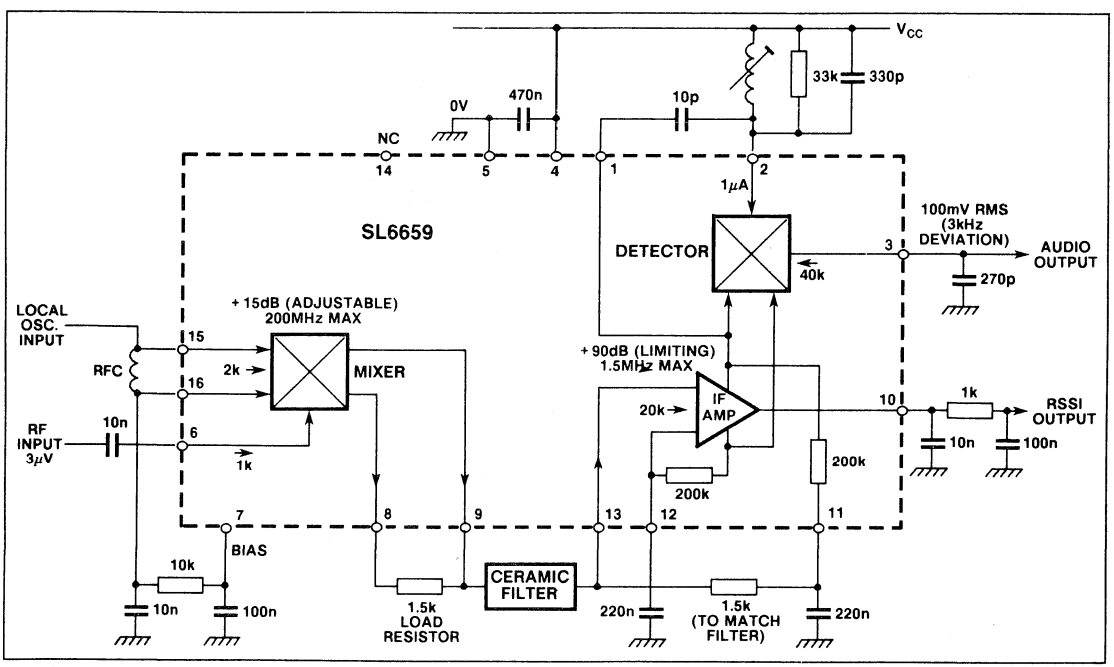


Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55°C to +150°C
Mixer input	1V rms

NOTE: This device has static sensitive inputs, sensitivity typically measured as 500V using MIL-STD-883 method 3015. Therefore, ESD handling precautions are essential to avoid degradation of performance or permanent damage of this device.

ELECTRICAL CHARACTERISTICS

The characteristics are guaranteed over the following conditions, unless otherwise stated:
V_{CC} = 2.5V to 7.5V, T_{AMB} = –30°C to + 85°C, IF = 455kHz, RF = 50MHz, Quad Coil working Q = 30

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	μV	20dB SINAD
		3		μV	12dB SINAD
AM rejection		40		dB	RF input <500μV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25°C
Co-channel rejection		7		dB	See Note 2
Mixer					
RF input impedance		1		kohm	
LO input impedance		2		kohm	
LO input bias		5		μA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
LO input level	180		300	mV	
LO frequency	200			MHz	
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	5mV into pin 13
Ultimate S/N ratio		60		dB	
THD		0.5	5	%	
Output impedance		40		kohm	
RSSI Output(T_{amb} = +25°C)					
Output current			25	μA	No input pin13
Output current	50		80	μA	Pin 13 = 2.5mV
Current change	0.9	1.22	1.5	μA/dB	See Note 1
Linear dynamic range	70			dB	See Note 1

NOTES
1. The RSSI output is 100% dynamically tested at 5V and + 20°C over a 70dB range. First the input to pin 13 is set to 2.5mV and the RSSI current recorded. Then, for each step of 10dB from –40 to + 30dB, the current is measured. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.
2. Co-channel rejection is measured by applying a 3kHz deviation, 1kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation, 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.

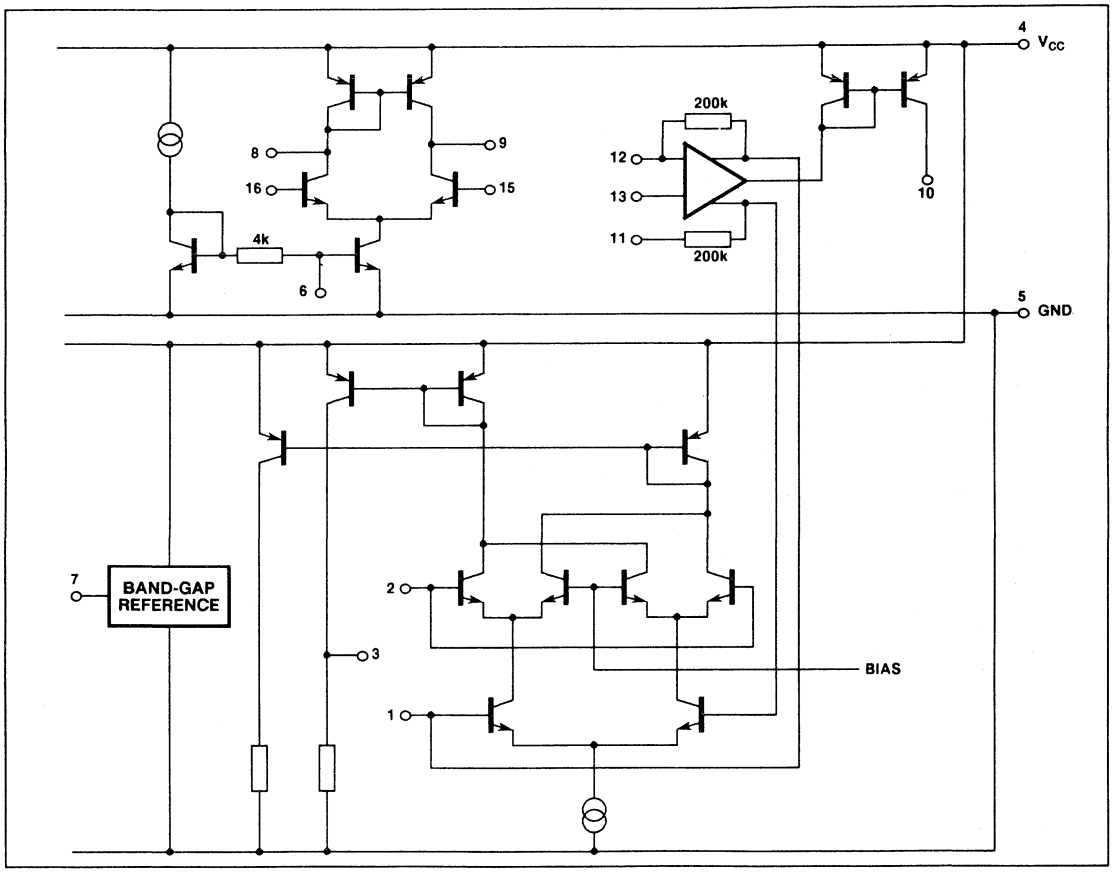


Fig.3 Internal schematic

GENERAL DESCRIPTION

The SL6659 is a very low power, high performance integrated circuit intended fo IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 200MHz
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with AF output
- An RSSI (Received Signal Strength Indicator) output

Mixer

The Mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The LO input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the local oscillator input.

IF Amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the ceramic filter. Because of the high gain, pins 11 and 12 must be adequately bypassed.

Detector

A conventional quadrature detector providing audio output is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network.

RSSI Output

The RSSI output is a current source with value proportional to the logarithm of the IF signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.

Supply Voltage

The SL6659 will operate reliably from 2.5V to 7.5V. The supply line must be decoupled with 470nF using short leads.

Internal Bias Voltage

The internal band-gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14Ω.

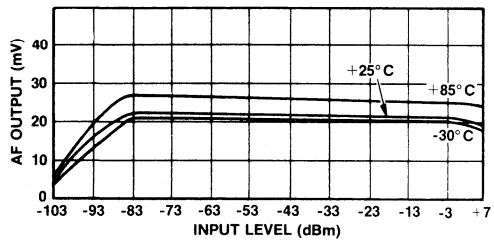


Fig.4 Audio output vs input and temperature at 2.5V

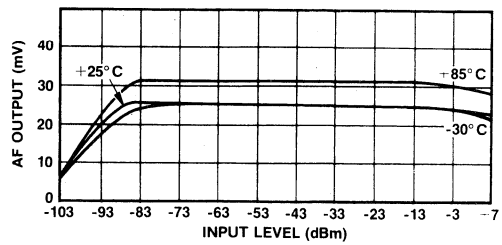


Fig.5 Audio output vs input and temperature at 5.0V

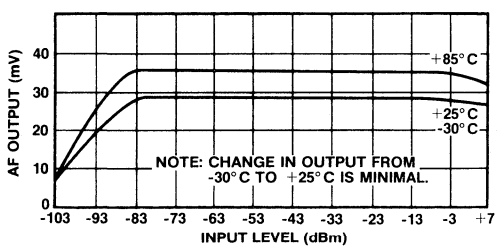


Fig.6 Audio output vs input and temperature at +7.5V

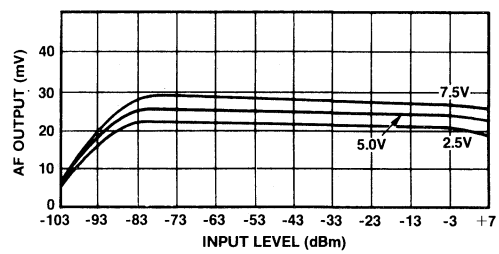


Fig.7 Audio output vs input and supply voltage at +25°C

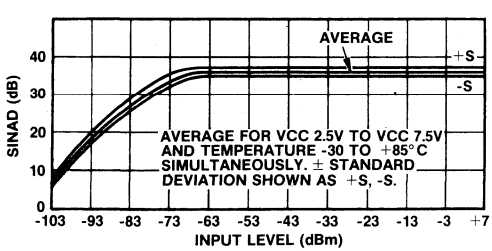


Fig.8 SINAD and input level

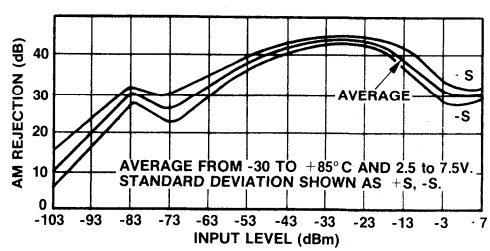


Fig.9 AM rejection and input level

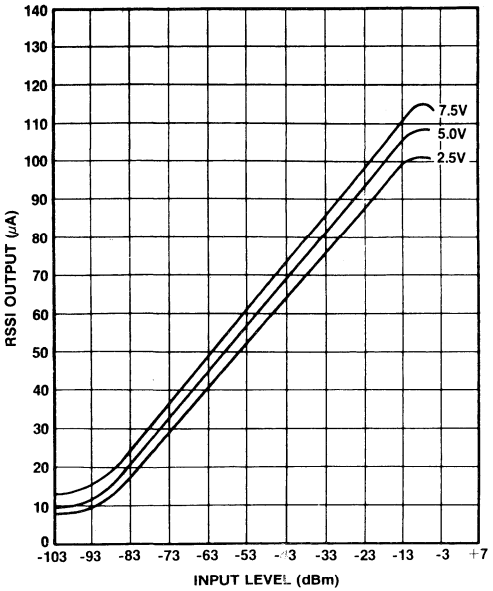


Fig.10 RSSI output vs input and supply voltage (T_{amb} = 20° C)

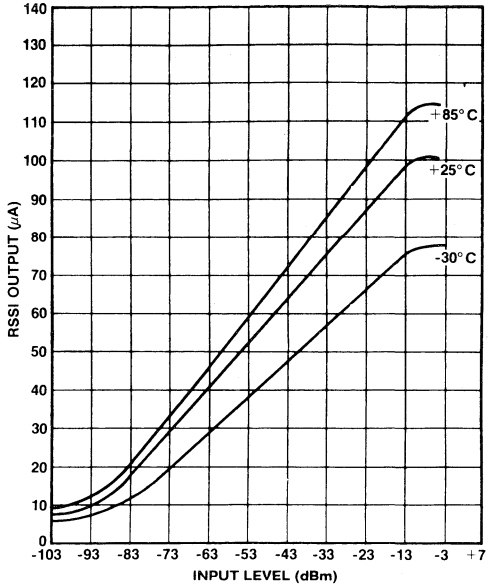


Fig.11 RSSI output vs input level and temperature (V_{CC} = 2.5V)

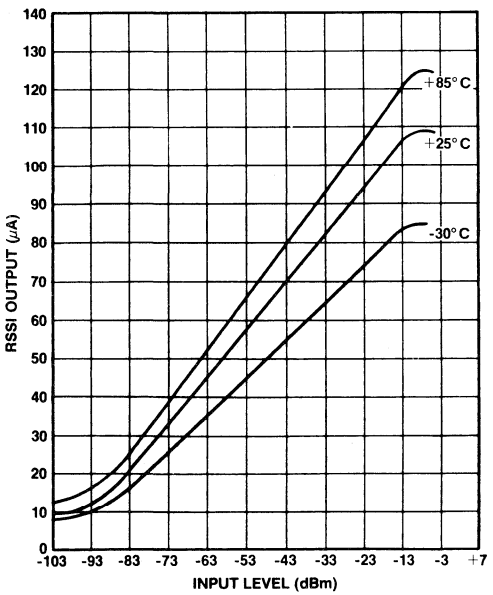


Fig.12 RSSI output vs input level and temperature (V_{CC} = 5V)

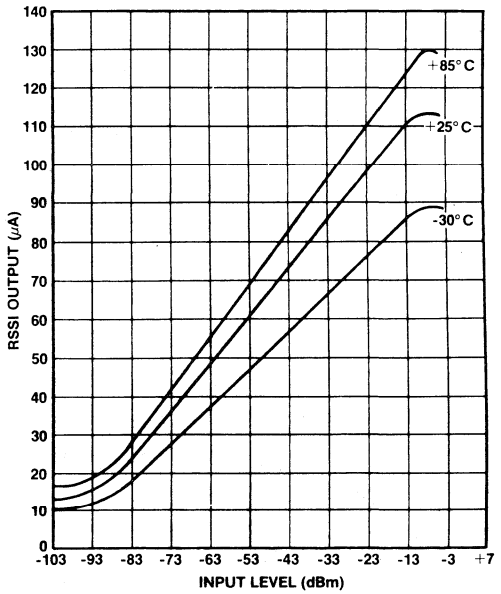


Fig.13 RSSI output vs input level and temperature (V_{CC} = 7.5V)

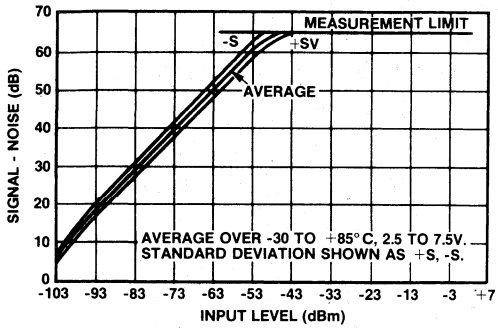


Fig.14 Signal + noise to noise ratio vs input level

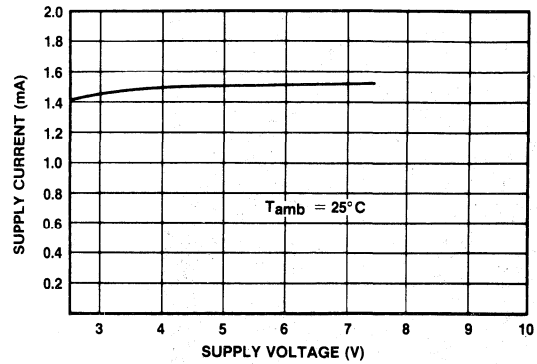


Fig.15 Supply current vs supply voltage

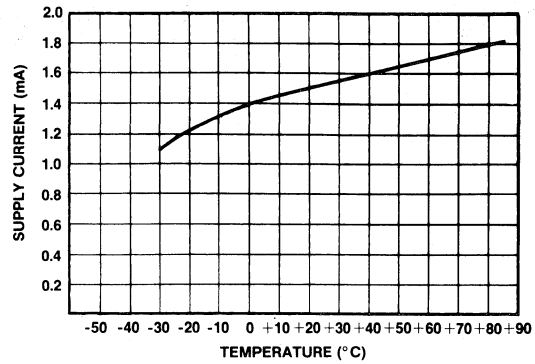


Fig.16 Supply current vs temperature (V_{CC} = 5V)

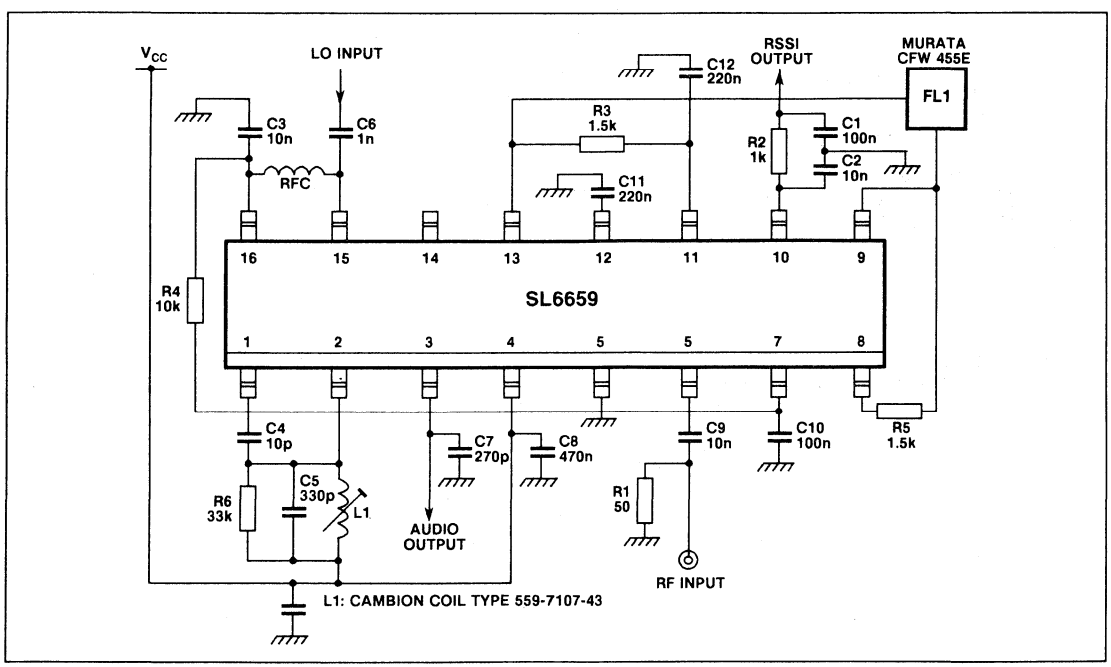


Fig.17 Circuit diagram of SL6659 demonstration board.

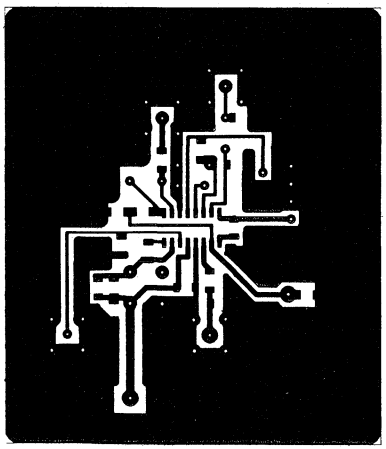


Fig.18 Track side of demonstration board.

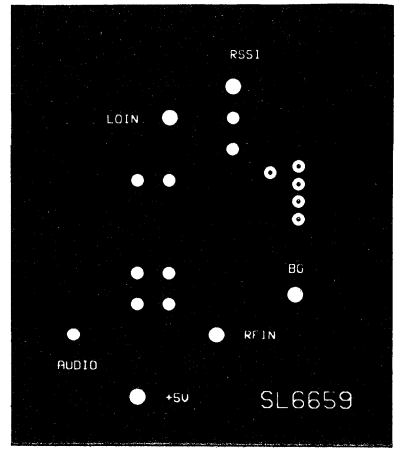


Fig.19 Ground plane of demonstration board.

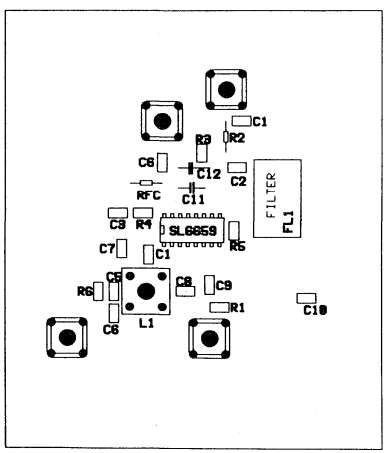


Fig.20 Component overlay of demonstration board viewed from track side.

COMPONENT LIST

R1	51Ω*	C4	10p*	FL1	CFW 455 E (MURATA)
R2	1kΩ	C5	330p*	L1	330μH (Adjustable) CAMBION TYPE 553-7107-43
R3	1.5kΩ*	C6	10n*		
R4	10kΩ*	C7	270p*		
R5	1.5kΩ*	C8	470n*		
R6	33kΩ*	C9	10n*	RFC	4.7μH
C1	100n*	C10	100n*		
C2	10n*	C11	220n		
C3	10n*	C12	220n		

Components marked thus: * are surface mounted on the track side

SP8703

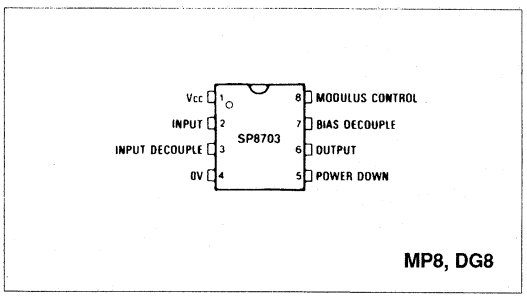
1GHz LOW CURRENT TWO-MODULUS DIVIDER

The SP8703 is a divide by 128/9 programmable divider with a maximum specified operating frequency of 1GHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The output stage is CMOS compatible only, the 0 to 1 output edge giving best loop delay performance.

A unique 'power-down' feature is included to minimise power consumption.



MP8, DG8

Figure 1 Pin connections - top view

FEATURES

- DC to 980MHz Operation
- -30°C to +70°C Temperature Range
- Unique Power-Down Feature
- CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.0V ± 0.25V
- Supply Current 30mA Typical

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6V
Storage temperature range	-30°C to +150°C
Max. Junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

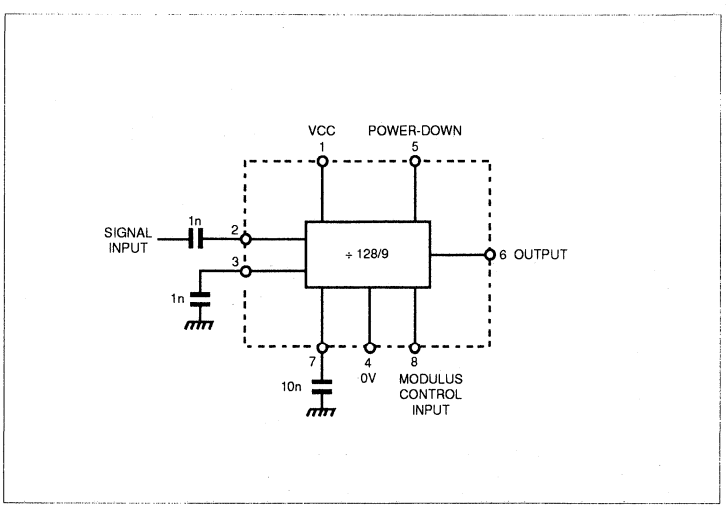


Figure 2 : Functional diagram SP8706

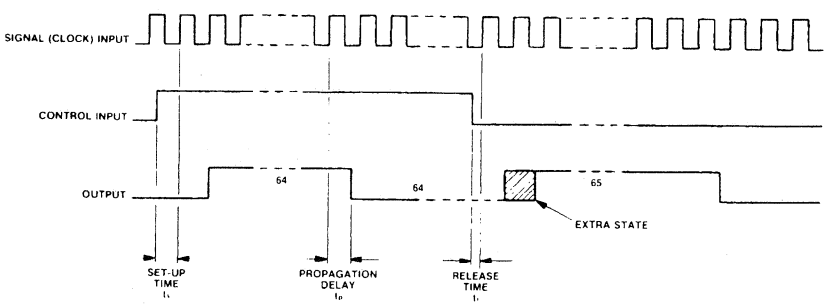
ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):]

VCC = +4.75V to 5.25V, Tamb = -30°C to +70°C

Characteristics	Value		Units	Conditions	Notes
	Min.	Max.			
Maximum frequency	1000		MHz	Tamb = 25°C	Note 1,2,4
Maximum frequency	950		MHz		Note 1,2,3
Maximum frequency (sinewave)		50	MHz		Note 1,2,3
Power supply current		40	mA	Power-up	Note 3
Power supply current		3	mA	Power-down	Note 3
Output high voltage	3.2	Vcc	V	IL = -0.2mA	Note 3
Output low voltage	0	1.7	V	IL = 0.2mA	Note 3
Control input high voltage	3.2	Vcc	V	Divide by 128	Note 3
Control input low voltage	0	1.7	V	Divide by 129	Note 3
Control input high current		50	µA	Input = Vcc	Note 3
Control input low current	-10		µA	Input = 0V	Note 3
Power-down high voltage	3.2	Vcc	V	Power-down	Note 3
Power-down low voltage	0	1.7	V	Power-up	Note 3
Power-down high current		10	µA	Input = Vcc	Note 3
Power-down low current	-2		µA	Input = 0V	Note 3
Clock to output delay		30	ns	CL = 10pF	Note 5
Set-up time		15	ns	CL = 10pF	Note 5
Release time		15	ns	CL = 10pF	Note5

NOTES
1. See Fig.4 for guaranteed operating window.
2. See Fig.5 for input voltage measurement method
3. Tested at 25°C and +70°C only
4. Tested at 25°C only
5. Guaranteed but not tested

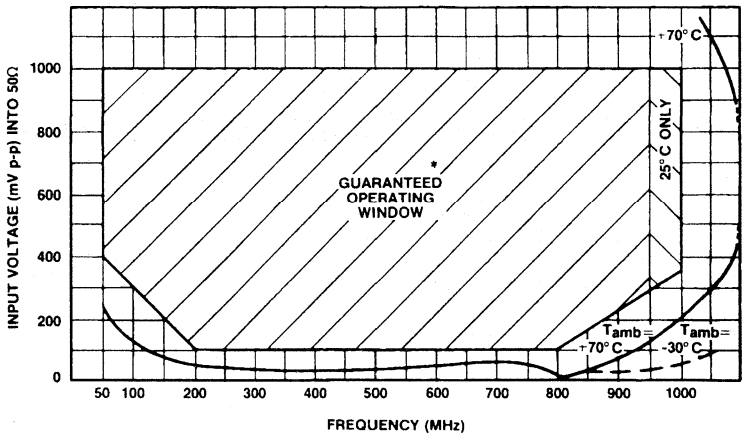


NOTE

The set-up time ts is defined as the minimum time that can elapse between a L → H transition of the control input and the next L → H clock pulse transition to ensure that the ÷ 128 mode is obtained.

The release time tr is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure that the ÷ 129 mode is obtain

Figure 3 : Timing diagram



* Tested as specified in table of Electrical Characteristics

Figure 4 : Typical input characteristics

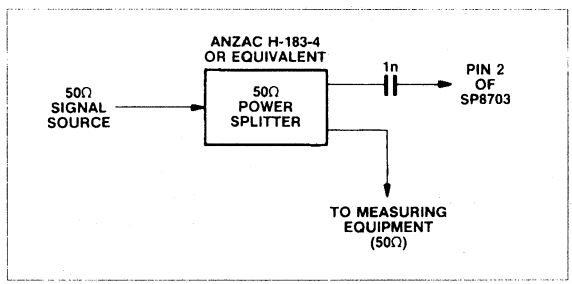


Figure 5 : Input voltage measurement method

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/lls.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.

DS 3289 -1

SP8704

950MHz VERY LOW CURRENT MULTI-MODULUS DIVIDER

The SP8704 is a switchable divide by 128/129, 64/65 programmable divider with a maximum specified operating frequency of 950MHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The SP8704 will operate from any supply from 3V to 5V and features full electrostatic discharge protection.

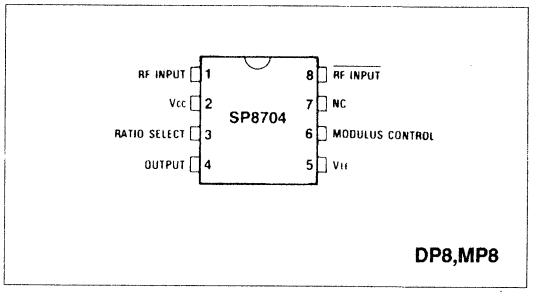


Fig. 1 Pin connections - top view

FEATURES

- DC to 950MHz Operation
- -40°C to +85°C Temperature Range
- Operation from 3V to 5V Supply
- ESD Protection on all Pins

QUICK REFERENCE DATA

- Supply Voltage 3V to 5V
- Supply Current 10mA - Including Output Emitter Follower

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V
Storage temperature range	-55°C to +125°C
Junction temperature	+175°C
Input voltage	2.5V p-p

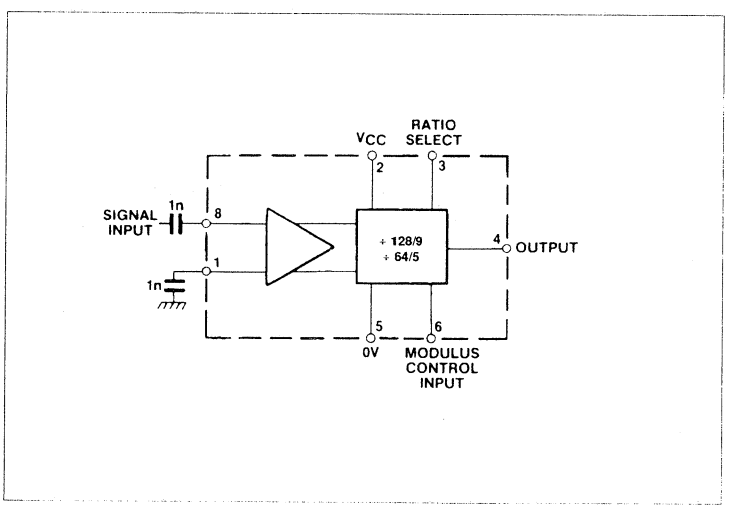


Fig. 2 Functional diagram SP8704

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to 85°C, VCC = +2.75V to +5.5V

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current			10		mA	Including output emitter follower
Input sensitivity	10MHz			150	mV rms	Sinewave input into 50Ω
	80MHz			25		
	150MHz			15		
	850MHz			15		
	950MHz			50		
Input impedance			50		Ω	
			2		pF	
Output			1		V pk-pk	Emitter follower output current source = 0.75mA
Ratio select (pin 3)	LO			1	V	128/129 selected
	HI	V_{cc}			V	64/65 selected
Modulus control (pin 6)	LO			1	V	65 or 129 selected
	HI	2			V	64 or 128 selected
Clock to output delay			8		ns	
Set up time			16		ns	
Release time			16		ns	

TRUTH TABLE

Pin 3	Pin 6	Division ratio
L	L	129
L	H	128
H	L	65
H	H	64

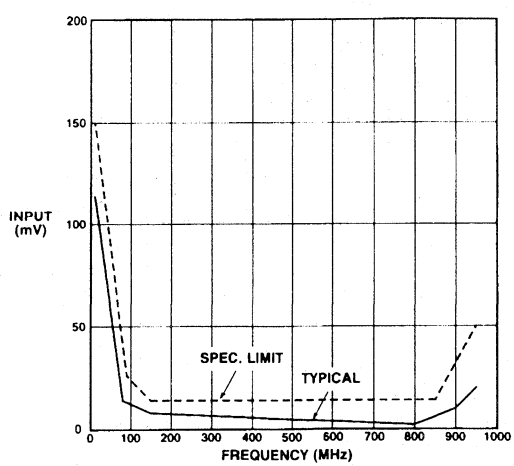


Fig. 3 Typical input sensitivity at 85°C

DS2416-2.3

SP8705

1100MHz VERY LOW CURRENT MULTI-MODULUS DIVIDER

(Supersedes October 1991 edition)

The SP8705 is a switchable divide by 128/129, 64/65 programmable divider with a maximum specified operating frequency of 1100MHz.

The signal (clock) inputs are biased internally and require to be capacitively coupled.

The SP8705 will operate from a supply of 3·3V to 5·5V and features electrostatic discharge protection on all pins.

FEATURES

- DC to 1100MHz Operation
- −40°C to +85°C Temperature Range
- Operation from a Single 3·3V to 5·5V Supply
- ESD Protection on All Pins

QUICK REFERENCE DATA

- Supply Voltage: 3·3V to 5·5V
- Supply Current: 5·6mA Max.

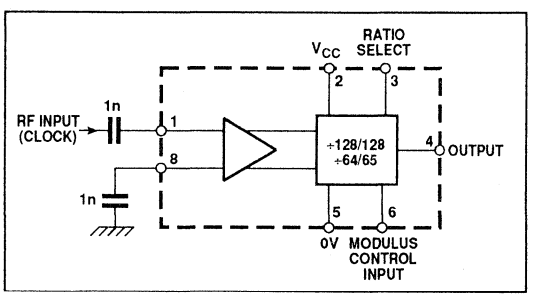


Fig. 2 Functional diagram of SP8705

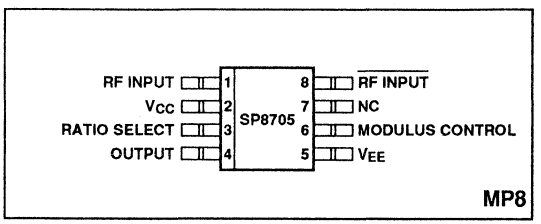


Fig. 1 Pin connections - top view

ORDERING INFORMATION

SP8705 NA MP (Miniature Plastic DIL Package)

ABSOLUTE MAXIMUM RATINGS (Note 1) (Non-simultaneous)

Supply voltage, V_{CC}	−0·5V to+ 7V (note 2)
Modulus control input	−0·5V to+6·0V (note 2)
Ratio select input	−0·5V to+6·0V (note 2)
Operating temperature range, T_{OP}	−40°C to +85°C
Storage temperature range, T_{STG}	−55°C to +150°C
Junction temperature	+150°C

NOTES

1. Stresses above those listed may cause permanent damage to the device. These are stress ratings only and functional operation at these conditions or at any other condition above those indicated in the Electrical Characteristics is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. Duration <1 hour.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, device performance is guaranteed over the following conditions:

V_{CC} = 3·3V to 5·5V, operating temperature = −40°C to +85°C (see note 3).

Characteristic	Value			Units	Conditions	Notes
	Min.	Typ.	Max.			
Supply current	-	4·75	5·60	mA	V_{CC} = 5·5V	
RF Input (clock) voltage range	70	-	1500	mVp-p	200-1000MHz	4
	100	-	1000	mVp-p	1000-1100MHz	4
Modulus Control input high	2·0	-	-	V	Divide by 64 or 128	
Modulus Control input low	-	-	0·8	V	Divide by 65 or 129	
Ratio Select input high	V_{CC}	-	-	V	Divide by 64 or 65	5
Ratio Select input low	-	-	0·8	V	Divide by 128 or 129	
Output voltage swing	0·6	1·5	-	Vp-p	R_L = 10kΩ, C_L = 12pF (see Fig. 7)	
Modulus set-up time,t_S	44	-	-	ns	See Fig. 5, f_{IN} = 500MHz	6, 7
Modulus release time, t_r	-	-	12	ns	See Fig. 5	7

NOTES

3. All electrical testing is performed at +85°C
4. The SP8705 will operate at input frequencies down to 10MHz with higher minimum input level.
5. Connect Ratio Select to V_{CC} for divide by 64/65 operation.
6. The modulus set-up time, t_s, is a function of frequency, the typical value being 2 clock cycles +40ns.
7. These parameters are not tested.

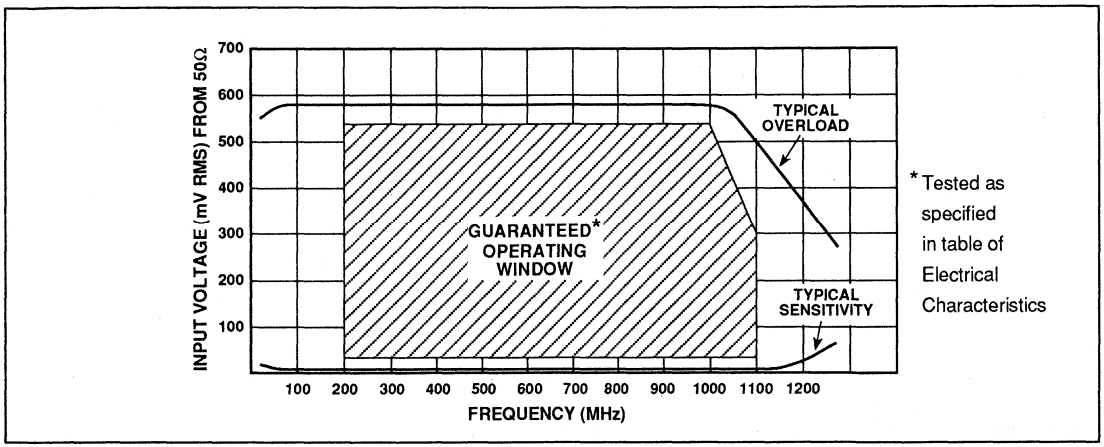


Fig. 3 Typical input characteristics

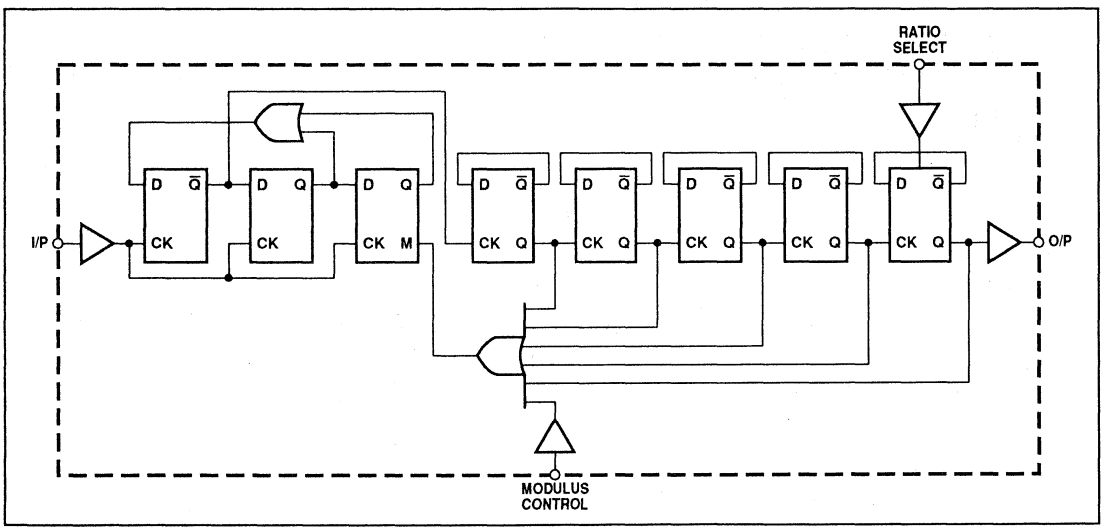


Fig. 4 SP8705 block diagram

OPERATING NOTES

The inputs are biased internally and coupled to a signal source with suitable capacitors.

The circuit will operate down to DC but slew rate must be better than 100V/µs.

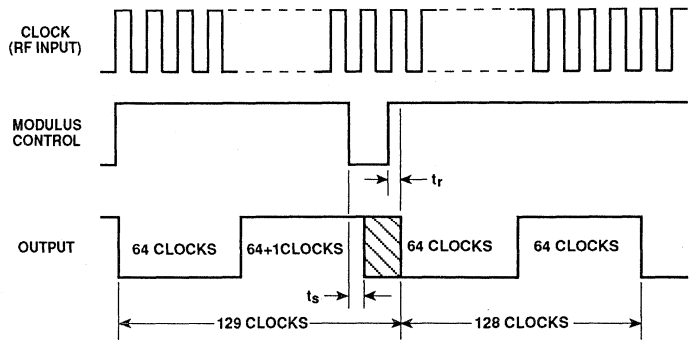
The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.

The SP8705 is NOT suitable for driving TTL or its derivatives.

If pin 3 (Ratio Select) is left open-circuit it will pull low (÷128/129 mode).

Ratio Select (pin 3)	Modulus Control (pin 6)	Division ratio
L	L	129
L	H	128
H	L	65
H	H	64

Table 1 Truth table



t_S, the modulus set-up time, is the minimum time required between Moulus Control going low and the next output falling edge, in order to ensure an N+1 modulus change.

t_r, the modulus release time, is the maximum time allowed between Modulus Control going high and the next output falling edge in order to maintain the N to N+1 modulus change for that output cycle.

Fig. 5 Modulus Control timing diagram

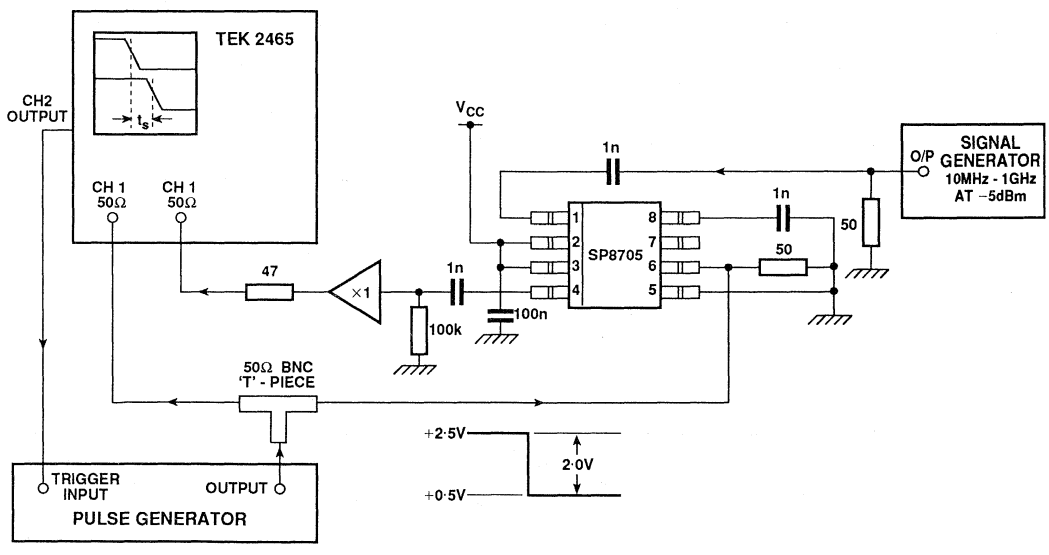


Fig. 6 Test circuit for set-up and release time measurement

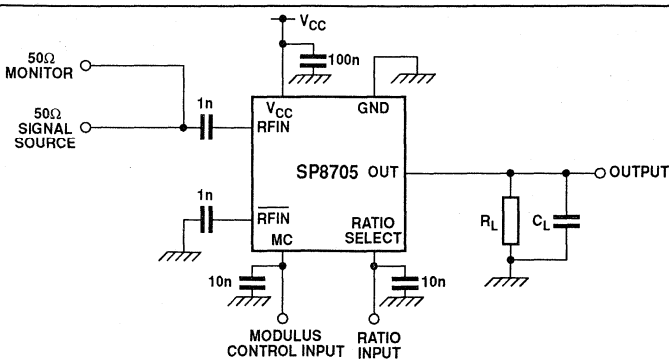


Fig. 7 Toggle frequency test circuit

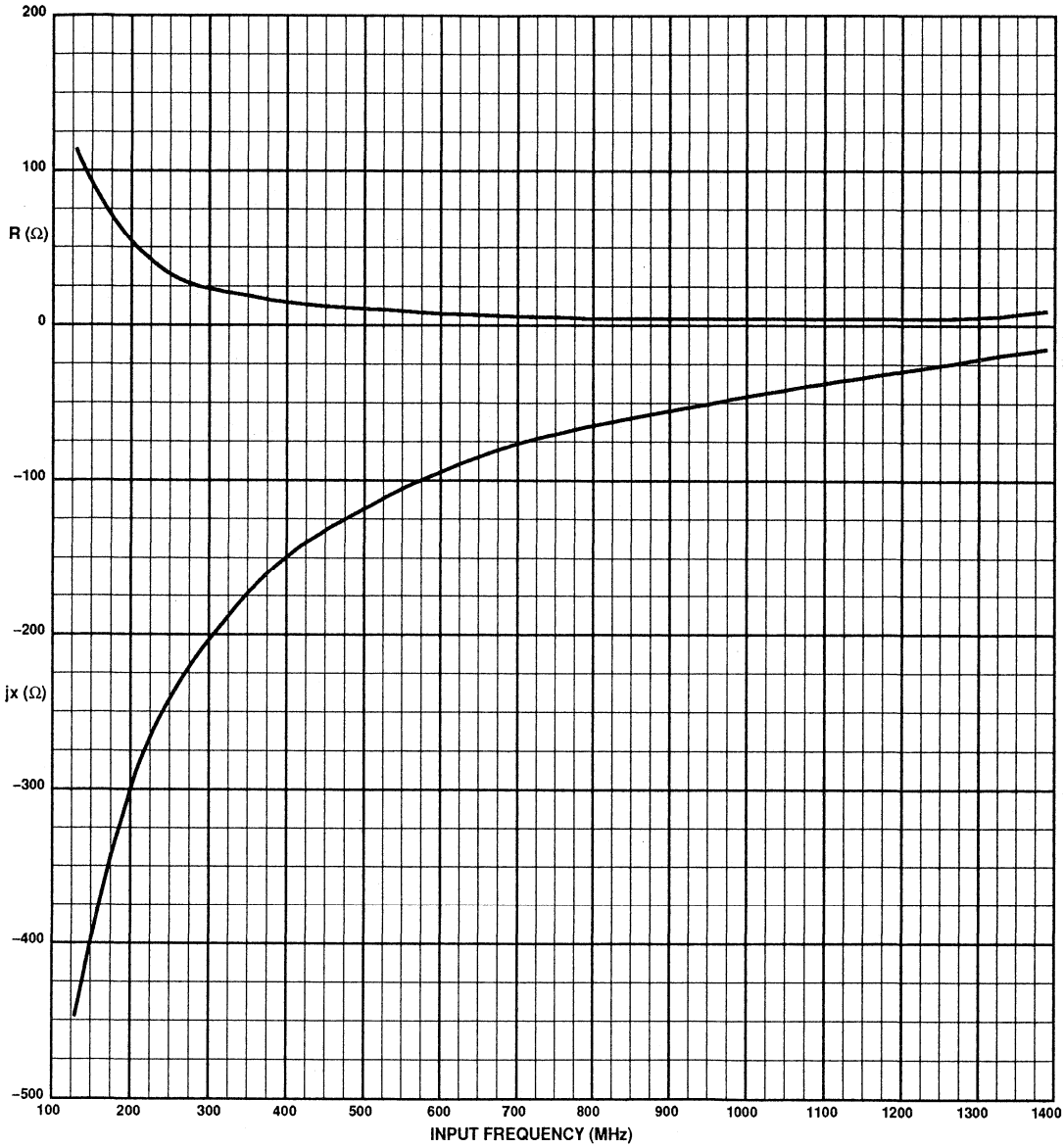
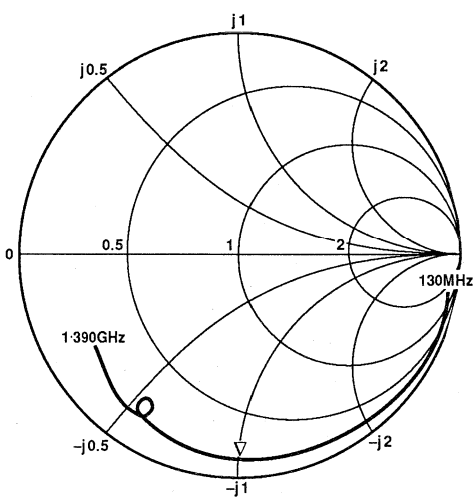


Fig. 8 Typical input impedance v. frequency

Frequency (GHz)	R (Ω)	–jx (Ω)
0·130	114.42	–449·08
0·162	77·16	–372·17
0·193	54·59	–314·30
0·225	47·69	–266·72
0·256	32·02	–236·62
0·288	25·45	–210·46
0·319	21·76	–189·13
0·351	18·07	–171·21
0·382	14·26	–156·68
0·414	13·70	–143·65
0·445	12·18	–133·35
0·477	11·52	–124·20
0·508	11·34	–114·27
0·540	10·29	–107·07
0·571	8·80	–99·81
0·603	8·11	–94·33
0·634	7·31	–89·23
0·666	7·11	–83·46
0·697	6·63	–78·67
0·729	6·34	–74·56
0·760	6·13	–70·51

Frequency (GHz)	R (Ω)	–jx (Ω)
0·792	5·80	–66·72
0·823	5·34	–62·87
0·855	5·41	–59·00
0·886	5·35	–56·23
0·918	5·10	–52·92
0·949	4·55	–49·89
0·981	4·75	–47·46
1·012	4·88	–44·66
1·044	4·84	–41·97
1·075	4·72	–39·32
1·107	4·80	–36·81
1·138	4·73	–34·35
1·170	4·99	–31·85
1·201	5·07	–29·21
1·233	6·19	–26·39
1·264	5·07	–26·74
1·296	5·45	–23·05
1·327	5·77	–20·21
1·360	8·81	–17·34
1·390	8·07	–14·32

Table 2 Coefficients for Fig. 8



V_{CC} = 5·5V, PLOT NORMALISED FROM 50Ω
MARKER ▽ AT 0·95GHz
Z_{IN} AT 0·95 GHz = 4·9Ω – j49·6Ω (DENORMALISED)

Fig. 9 Input impedance S_{11}

DS 3290 -1.0

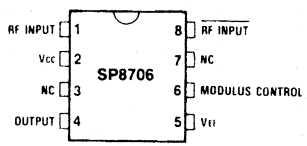
SP8706

980MHz LOW CURRENT TWO-MODULUS DIVIDER

The SP8706 is a divide by 80/81 programmable divider with a maximum specified operating frequency of 980MHz.

The signal (clock) inputs are biased externally and require to be capacitor coupled.

The SP8706 will operate from a supply of 5V.



MP8

Figure 1 Pin connections - top view

FEATURES

- DC to 980MHz Operation
- -40°C to +70°C Temperature Range

QUICK REFERENCE DATA

- Supply Voltage 4.5V to 5.5V
- Supply Current 20mA - Including Output Emitter Follower

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V
Storage temperature range	-55°C to +125°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8706 KG MPAS

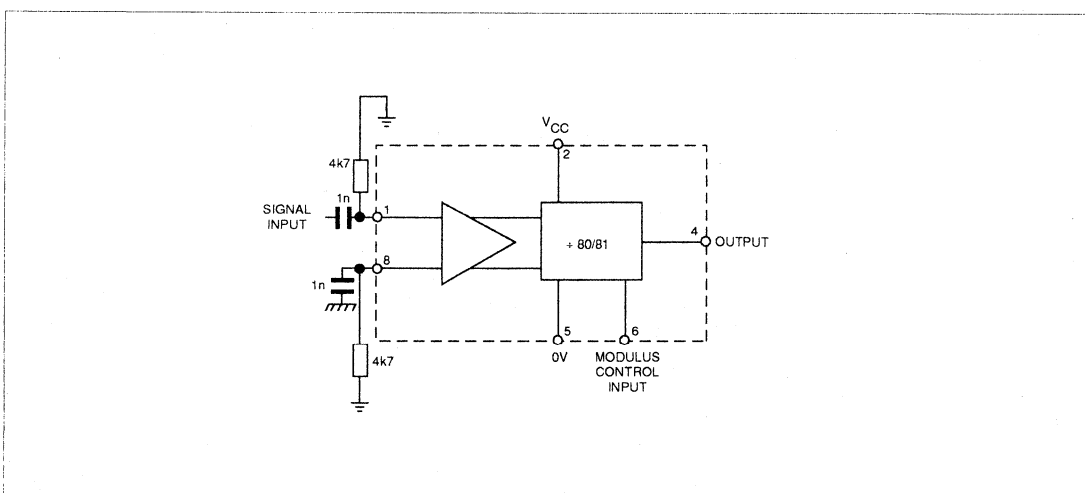


Figure 2 : Functional diagram SP8706

ABSOLUTE MAXIMUM CHARACTERISTICS & RATINGS

Symbol	Parameter	Min.	Max.	Units	Duration	Notes
V_{CC}	Supply Voltage	-0.5	7.0	V	<1Hr	
MC	Modulus Control Input	-0.5	6.0	V	<1Hr	
V_{IN}	RF Input Voltage	-	2.5	V p-p	-	1
T_{OP}	Operating Temperature	-40	70	°C	-	
T_{STG}	Storage Temeperature	-55	150	°C	-	

Stress above those listed may cause permanent damage to the device. This is a stress rating only and fuctional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablity.
NOTE1. Vin is the voltage measured differentially between RFINPUT and $\overline{\text{RFINPUT}}$.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, device performance is guaranteed over the following conditions:
Supply Voltage, Vcc 4.5V to 5.5V. Operating Temperature -40°C to +70°C

Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
Supply Current	V_{CC} = 5.5V	-	14	20	mA	1
Input Voltage Range	80-150MHz	25	-	500	mVrms	2
	150-750MHz	15	-	500	mVrms	
	750-850MHz	22	-	500	mVrms	
	850-980MHz	50	-	500	mVrms	
MOD Control Input HIGH	Divide by 80	2.0	-	-	V	
MOD Control Input LOW	Divide by 81	-	-	1.0	V	
Output Voltage Swing	R_L = 10K, C_L = 10pF	-	1.0	-	V p-p	
Modulus Set-up Time	See Fig. 3		26	-	nS	3
Modulus Hold Time	See Fig. 3	$1/F_{IN}$	-	-	Sec	3
Modulus Release Time	See Fig. 3	-	$t_h + t_S$	-	Sec	3

N.B. All electrical testing is performed at room temperature

Notes:
1. Includes external bias resistors.
2. The device will operate to 10MHz with higher minimum input level.
3. These parameters are not tested.

Pin	Pin Name	Description
1	RF Input	Must be AC coupled to RF source with suitable capacitor.
2	Vcc	4.5V to 5.5V with a typical supply current of 14mA. Must be well decoupled to Gnd.
4	Output	1V peak to peak output swing driving 10pF and 10K
5	VEE	Negative supply pin
6	Modulus Control	Low input (1V) gives divide by 81 High input (2V) gives divide by /80
8	$\overline{\text{RF Input}}$	Must be decoupled with suitable capacitor to the reference supply of the input signal. This may be Vcc for VCOs.

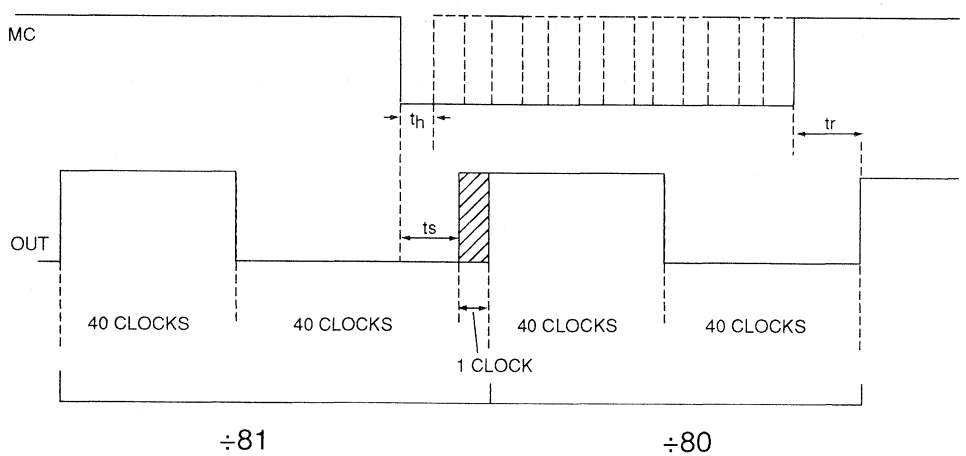
Table 1 : Pin Functions

OPERATING NOTES

1. The RF inputs are biased externally and coupled to a signal source with suitable capacitors.
2. The 4K7 RF input bias resistors must be matched to within ±1% of value.
3. The circuits will operate down to DC but slew rate must be better than 100V/µs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits should not be used.
5. This device is NOT suitable for driving TTL or its derivatives.

Pin 6	Division Ratio
L	81
H	80

Table 2 : Truth Table



t_s = The minimum time required between 'Modulus Control' going low and the next output rising edge, in order to ensure a P+1 modulus change.

t_h = The minimum time 'Modulus Control' must remain low to sustain the P + 1 modulus for that O/P period.

t_r = The minimum time allowed between 'Modulus Control' going high and the O/P rising edge in order to aviod a P + 1 modulus change in the following O/P cycle.

Figure 3 : Modulus Control Timing Diagram

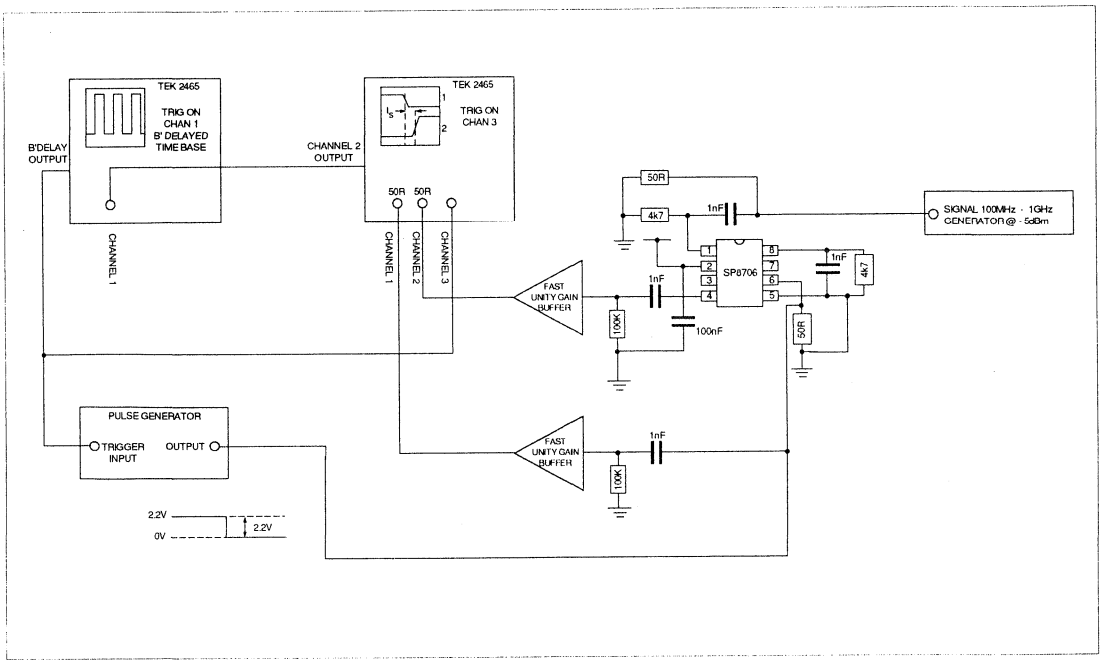


Figure 4 : Test circuit for setup and release time measurement

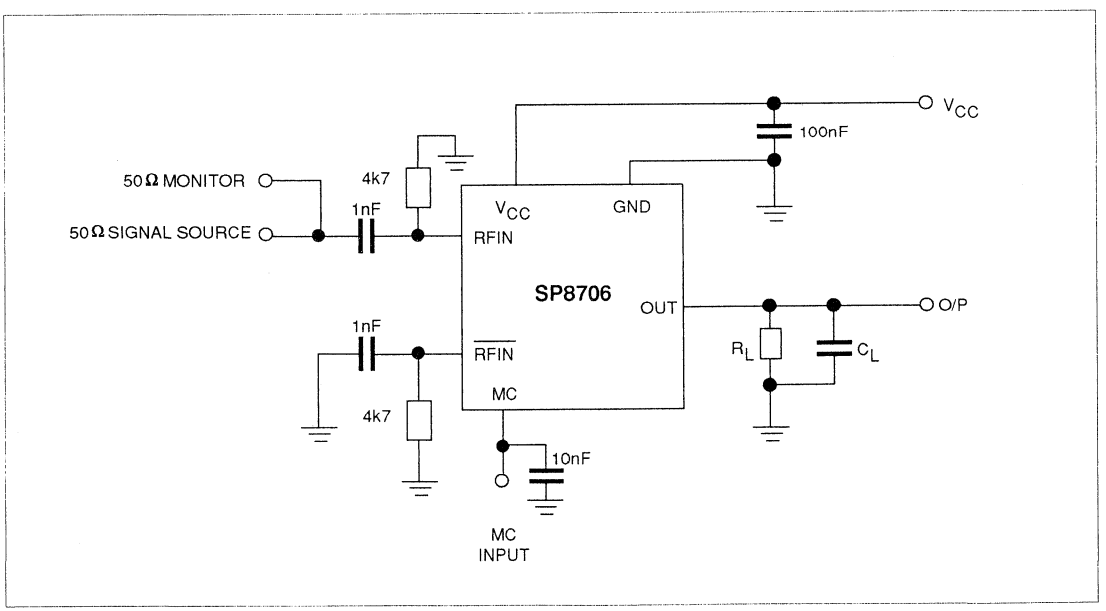
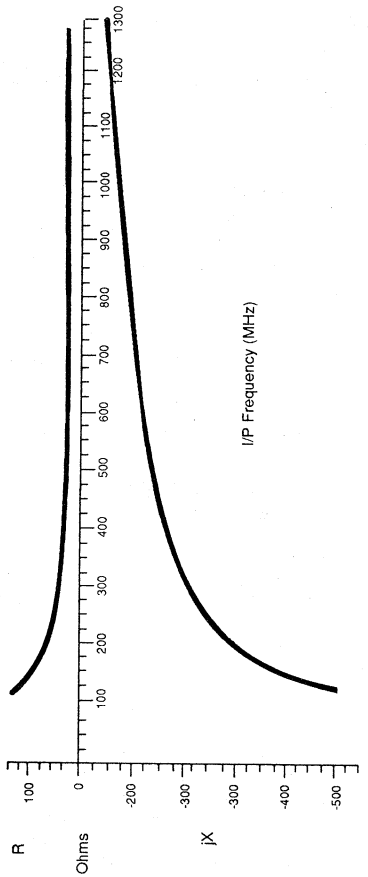


Figure 5 : Toggle Frequency Test Circuit



Freeuency (MHz)	R (Ω)	jX (Ω)
130	195	-351
156	133	-321
183	105	-281
209	78	-248
236	65	-223
262	55	-203
289	48	-185
315	42	-169
342	37	-156
368	33	-145
395	31	-136
421	27	-127
448	25	-119
474	23	-112
501	23	-106
527	21	-100
554	19	-94
580	18	-89
607	17	-85
633	17	-81
660	16	-77
686	15	-73
713	15	-70
739	14	-67
766	14	-64
792	13	-61
819	13	-58
845	13	-55
872	12	-53
898	12	-50
925	12	-48
951	12	-46
978	12	-44
1004	11	-42
1031	11	-39
1057	11	-37
1084	11	-36
1110	11	-34
1137	12	-33
1163	11	-31
1190	12	-29

Figure 6 : Typical Input impedance vs frequency

V_{CC} = 5.0V	Plot normalised from 50R
START	0.1300GHz
STOP	1.1900GHz
MARKER ↓	0.98GHz
Z_{IN} at 0.98GHz	12.15Ω - -j44.02Ω (de normalised)

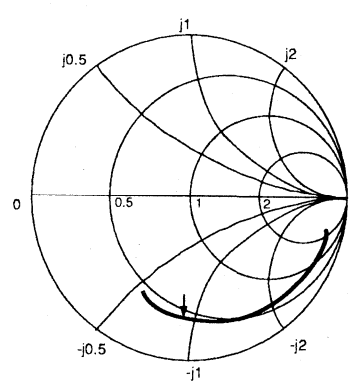


Figure 7 : SP8706MP Smith Chart S_{11} Measurement

DS3562-2.1

SP8714

2100MHz VERY LOW CURRENT MULTI-MODULUS DIVIDER

The SP8714 is a switchable divide by 32/33, 64/65 programmable divider with a maximum specified operating frequency of 2100MHz. The signal (clock) inputs are biased internally and require to be capacitively coupled.

The SP8714 will operate from a supply of 2·7V to 5·5V and features a power-down facility for battery economy.

FEATURES

- DC to 2100MHz Operation
- −40°C to +85°C Temperature Range
- Operation from a Single 2·7V to 5·5V Supply

QUICK REFERENCE DATA

- Supply Voltage: 2·7V to 5·5V
- Supply Current: 8·5mA Max. (Including O/P Current)

APPLICATIONS

- Digital Cordless Phones (DECT, JDCT)
- Japanese Digitial Cellular, DCS1800

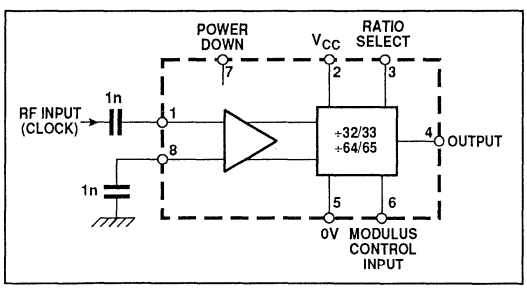


Fig. 2 Functional diagram of SP8714

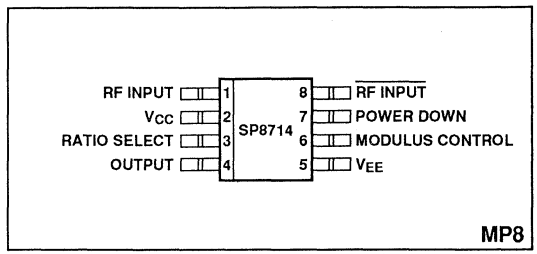


Fig. 1 Pin connections - top view

ORDERING INFORMATION

SP8714 IG MPAS (Industrial-Miniature Plastic DIL Package)

ABSOLUTE MAXIMUM RATINGS (Note 1) (Non-simultaneous)

Supply voltage, V_{CC}	−0·5V to+7V (note 2)
Modulus control input	−0·5V to+6·0V (note 2)
Ratio select input	−0·5V to+6·0V (note 2)
Power down input	−0·5V to+6·0V (note 2)
Operating temperature range, T_{OP}	−40°C to +85°C
Storage temperature range, T_{STG}	−55°C to+150°C
Junction temperature	+150°C

NOTES

1. Stresses above those listed may cause permanent damage to the device. These are stress ratings only and functional operation at these conditions or at any other condition above those indicated in the Electrical Characteristics is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. Duration <1 hour.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, device performance is guaranteed over the following conditions:

V_{CC} = 2·7V to 5·5V, operating temperature = −40°C to+85°C (see note 3).

Characteristic	Value			Units	Conditions	Notes
	Min.	Typ.	Max.			
Supply current	-	6·5	8·5	mA	V_{CC} = 5·5V	
RF Input (clock) voltage range	50		200	mVrms	100-2100MHz	4
Modulus Control input high	$0{\cdot}6V_{CC}$	-	-	V	Divide by 32 or 64	4
Modulus Control input low	-	-	$0{\cdot}4V_{CC}$	V	Divide by 33 or 65	
Ratio Select input high	$0{\cdot}6V_{CC}$	-	-	V	Divide by 32 or 33	5
Ratio Select input low	-	-	$0{\cdot}4V_{CC}$	V	Divide by 64 or 65	
Power Down input high	$V_{CC}-1{\cdot}0$	-	-	V	Powered down	
Power Down input low	-	-	$V_{CC}-2{\cdot}0$	V	Powered up	
Output voltage swing	500	-	-	mVp-p	C_L = 10pF (see Fig. 6)	
Modulus set-up time, t_s	-	1	-	ns	See Fig. 5	6, 7
Modulus hold time, t_h	-	1	-	ns	See Fig. 5	7

NOTES

3. All electrical testing is performed at +85°C. 4. The SP8714 will operate at input frequencies down to 10MHz with higher minimum input level. 5. Connect Ratio Select to V_{CC} for divide by 32/33 operation. 6.The modulus control is latched at the end of the previous cycle. 7. These parameters are not tested.

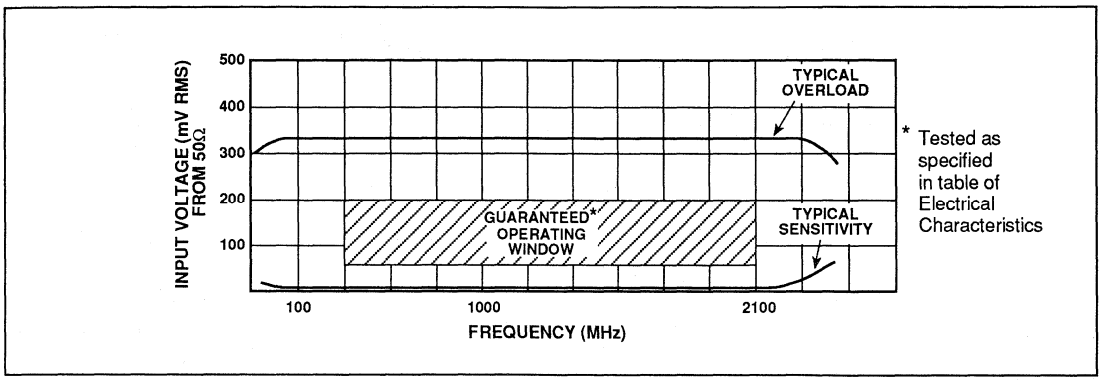


Fig. 3 Typical input characteristics

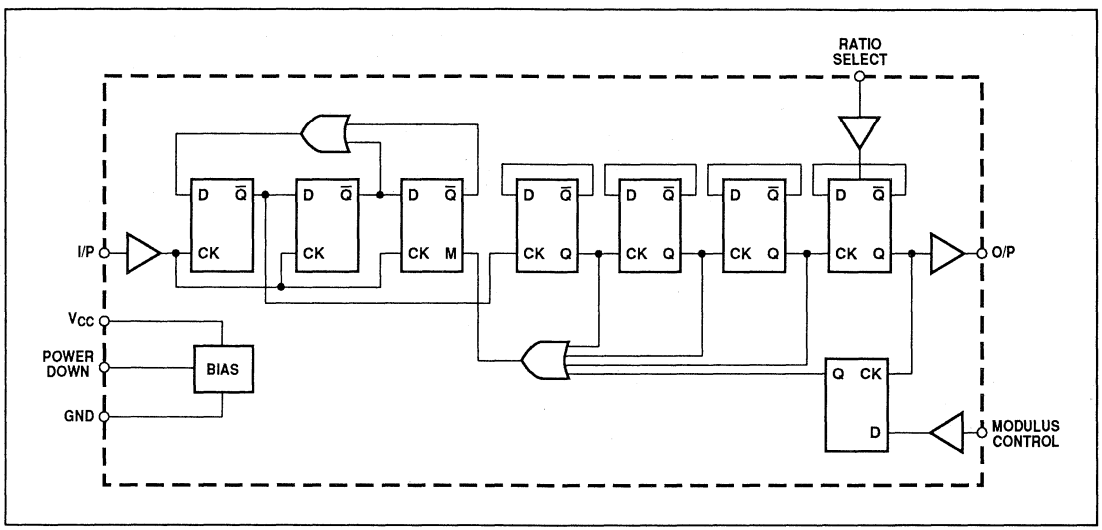


Fig. 4 SP8714 block diagram

OPERATING NOTES

The inputs are biased internally and coupled to a signal source with suitable capacitors.

The circuit will operate down to DC but slew rate must be better than 100V/μs.

The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.

The SP8714 is NOT suitable for driving TTL or its derivatives.

POWER DOWN (pin 7) should be tied to GND if not being used.

Ratio Select (pin 3)	Modulus Control (pin 6)	Division ratio
L	L	65
L	H	64
H	L	33
H	H	32

Table 1 Truth table

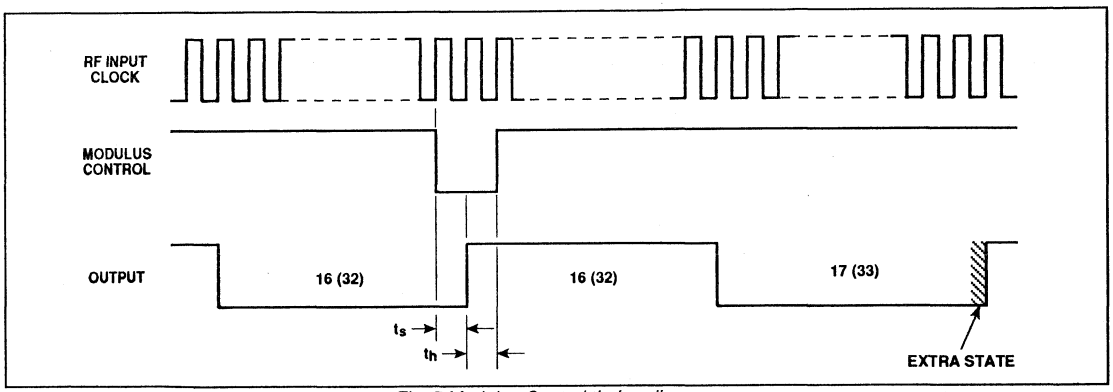


Fig. 5 Modulus Control timing diagram

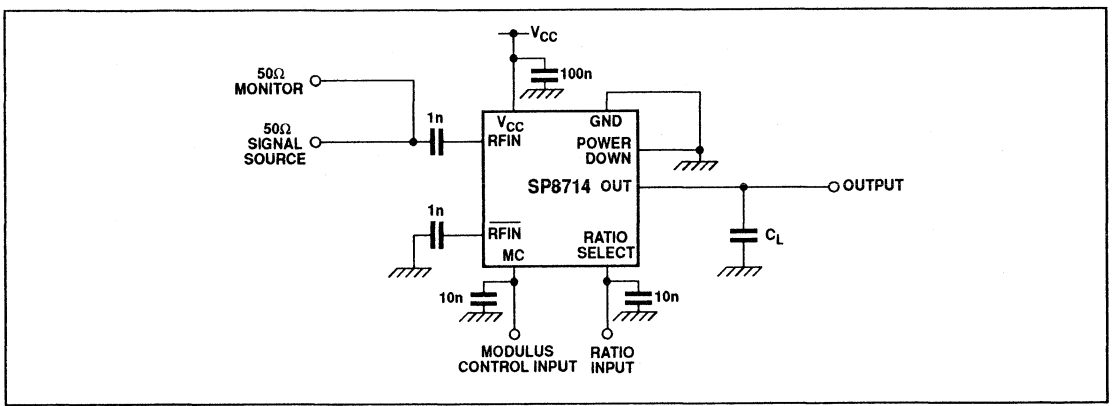


Fig. 6 Toggle frequency test circuit

DS 3292 -1

SP8716/8/9

520MHz LOW CURRENT TWO-MODULUS DIVIDERS

SP8716 ÷ 40/41, SP8718 ÷ 64/65, SP8719 ÷ 80/81 are 50mW programmable dividers with a maximum specified operating frequency of 520MHz over the temperature range -40 °C to + 85 °C.

The signal (clock) inputs are biased internally and require to be capacitor coupled. The output stage is of an unusual low power design featuring dynamic pull-up, and optimised for driving CMOS. The 0 to 1 output edge should be used to give the best loop delay performance.

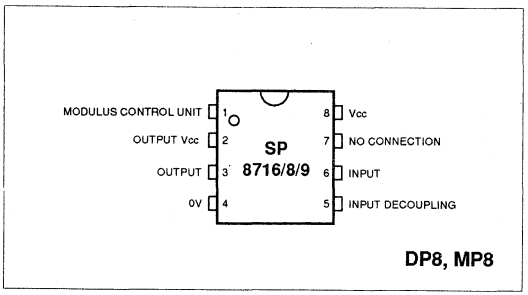


Figure : 1 Pin connections - top view

FEATURES

- DC to 520MHz Operation
- -40°C to +85°C Temperature Range
- Control Inputs and Outputs are CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.0V ± 0.25V
- Supply Current 10.5mA typ.

ABSOLUTE MAXIMUM RATINGS

Supply voltage pin 2 or 8):	8V
Storage temperature range:	-55°C to +150°C
Max. Junction temperature:	+175°C
Max. clock I/P voltage:	2.5V p-p

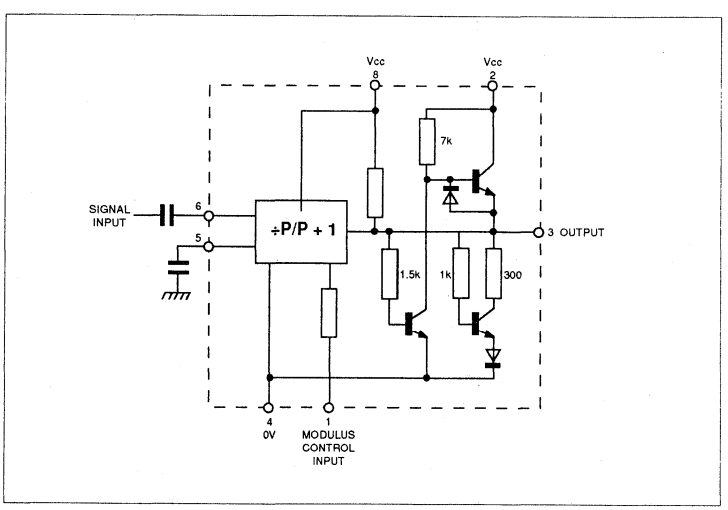


Figure 2 : Functional diagram

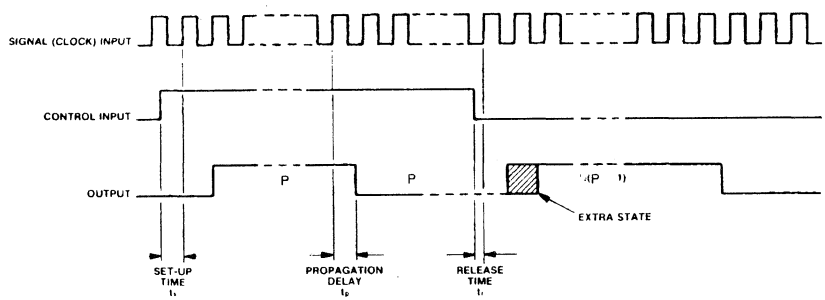
ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):]

Supply voltage: Vcc = +4/95 to 5.45V, Temperature: T_{amb} = -40°C to +85°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Max. frequency	f_{max}	520		MHz	Input 100-280mV p-p	1
Min. frequency (sinewave input)	f_{min}		30	MHz	Input 400-800mV p-p	2
Power supply current	I_{CC}		11.9	mA	C_L = 3pF; pins 2, 8 linked	1
Output high voltage	V_{OH}	(Vcc - 1.2)		V	I_L = -0.2mA	1
Output low voltage	V_{OL}		1	V	I_L = 0.2mA	1
Control input high voltage	V_{INH}	3.3	8	V	÷P	1
Control input low voltage	V_{INL}	0	1.7	V	÷P +1	1
Control input high current	V_{INH}		0.41	mA	V_{INH} = 8V	1
Control input low current	VINL	-0.20		mA	V_{INL} = 0V	1
Clock to output delay	t_p		28	ns	C_L = 10pF	2
Set-up time	t_s	10		ns	C_L = 10pF	2
Release time	t_r	10		ns	C_L = 10pF	2

NOTES
1. Tested at 25°C only
2. Guaranteed but not tested

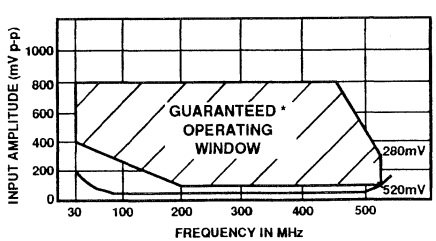


NOTE

The set-up time ts is defined as the minimum time that can elapse between a L → H transition of the control input and the next L → H clock pulse transition to ensure that the ÷P mode is obtained.

The release time tr is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure that the ÷(P +1) mode is obtain

Figure 3 : Timing diagram



*Tested as specified in table of Electrical Characteristics

Figure 4 : Typical input characteristics

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/,us.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.
5. This device is NOT suitable for driving TTL or its derivatives.

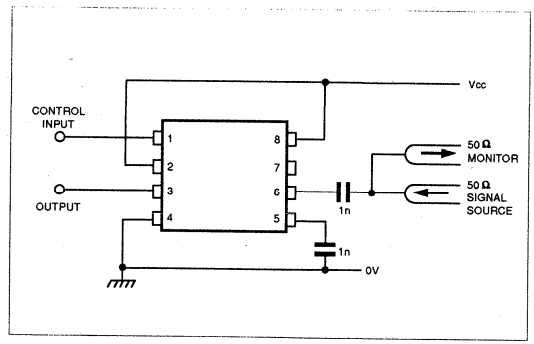


Figure 5: Toggle frequency test circuit

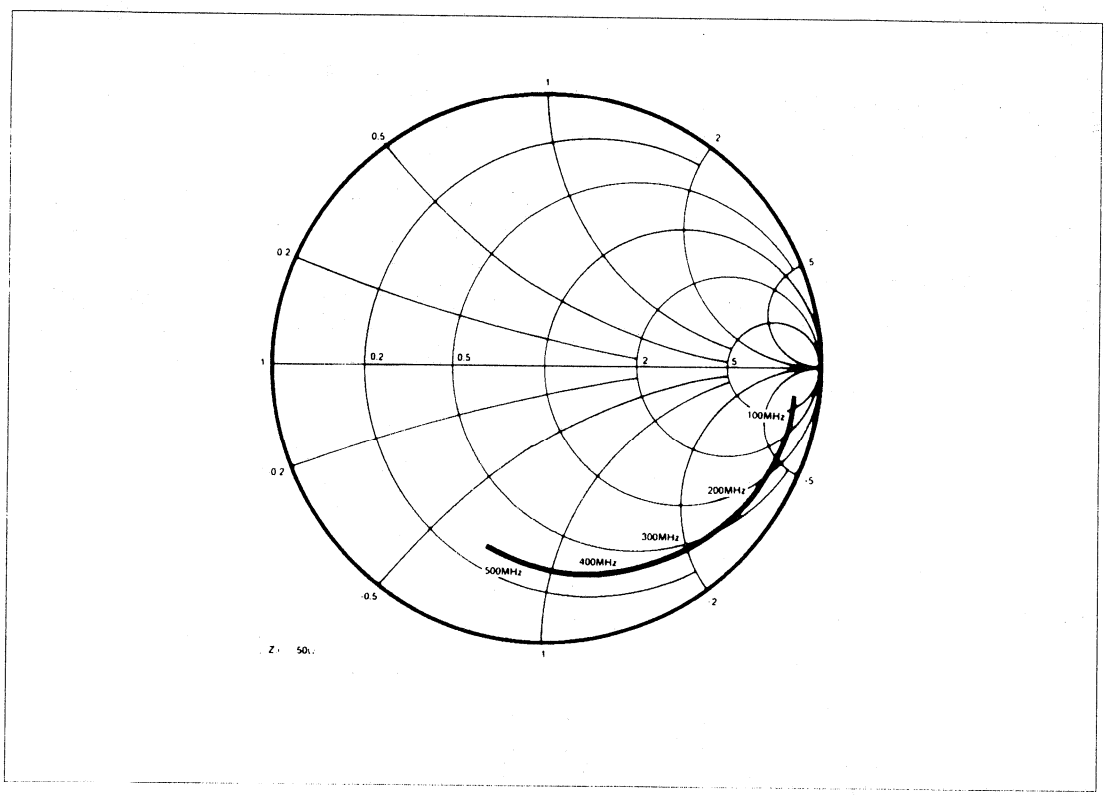


Figure 6 : Typical input impedance

SP8789

225MHz ÷ 20/21 TWO MODULUS DIVIDER

The SP8789 is a low power programmable ÷20/21 counter.It divides by 20, when the control input is in the high state and by 21 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

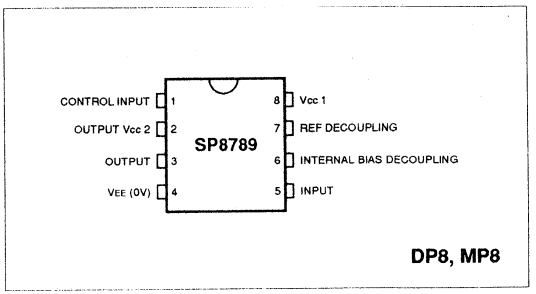


Figure 1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply Voltage 5.2V or 6.8V to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. Junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2	Max. 10V

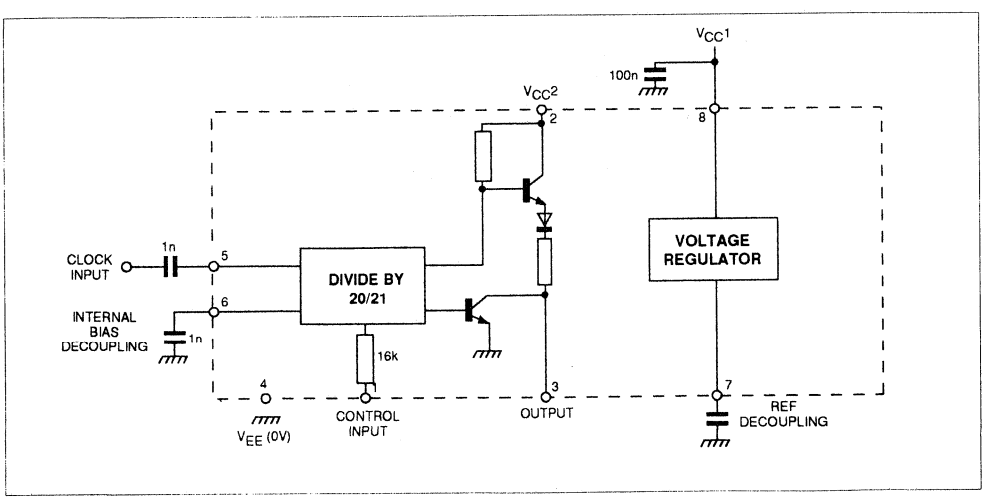


Figure 2 : Functional diagram SP8789

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):]

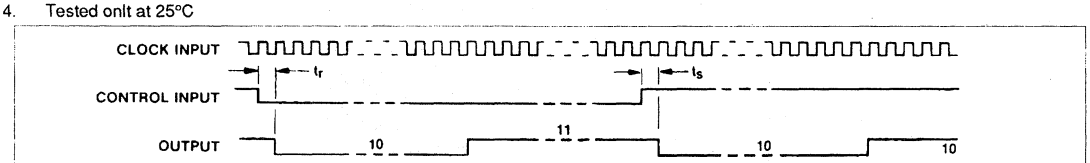
Supply voltage : Vcc 1 & 2 = 5.2 ± 0.25V or 6.8V to 9.5V (see Operating Note 7):

V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristics	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input))	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked Vcc = 4.95V I_{OH} = 100µA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES

1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested onlt at 25°C



TRUTH TABLE FOR CONTROL INPUTS

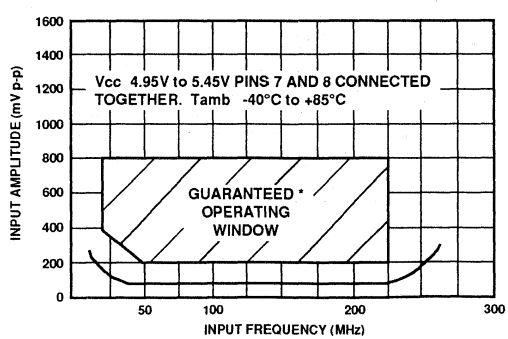
Control input	Division Ratio
0	21
1	20

Figure 3 : Timing diagramSP8789

NOTES

The set-up time ts is defined as the minimum time that can elapse between a L → H transition of the control input and the next L → H clock pulse transition to ensure that the ÷ 20 mode is selected.

The release time tr is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure that the ÷ 21 mode is selected.



*Tested as specified in table of Electrical Characteristics

Figure 4 : Input sensitivity SP8789

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector canbereturnedtoa +10Vlineviaa5kresistorbuttheoutput sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/~s is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

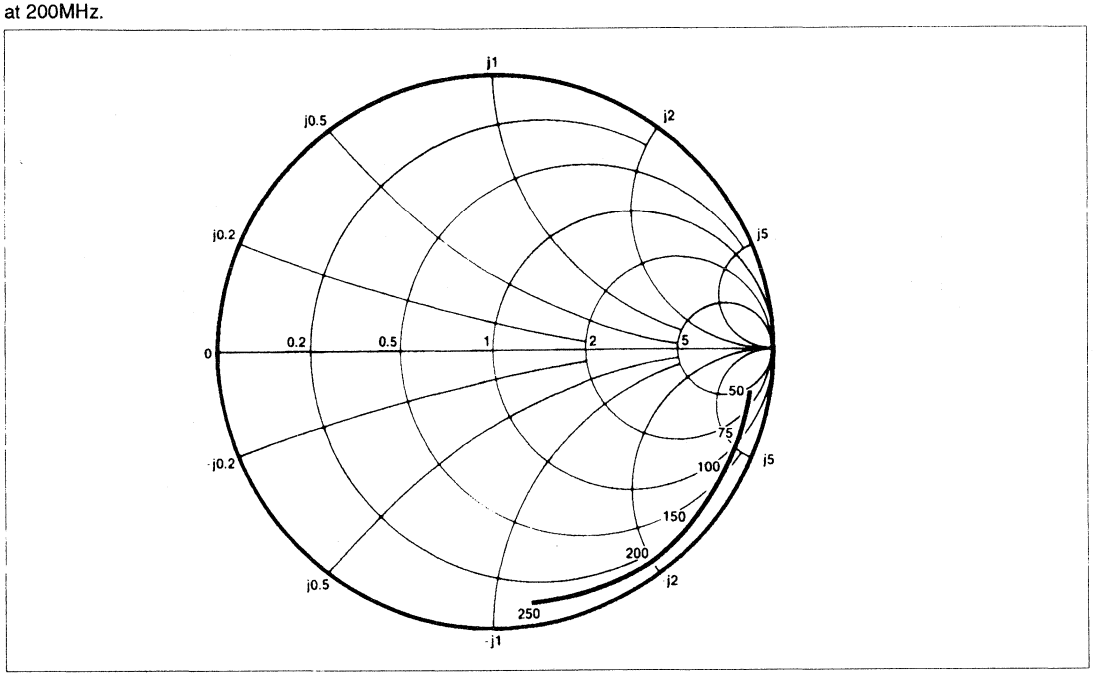


Figure 5 : Typical impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedance normalised to 50 ohms.

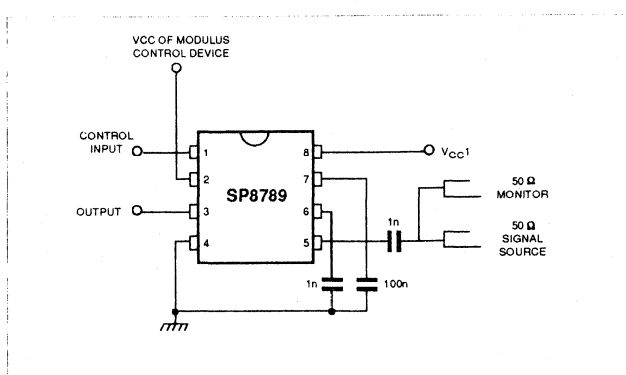


Figure 6 : Toggle frequency test circuit

DS 3294- 1

SP8792 225MHz ÷ 80/81
SP8793 225MHz ÷ 40/41
WITH ON-CHIP VOLTAGE REGULATOR

The SP8792 AND SP8793 are low power programmable ÷80/81 and ÷40/41 counter, temperature range: -40°C to +85°C.They divide by 80(40) when control input is in the high state and by 81(41) when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

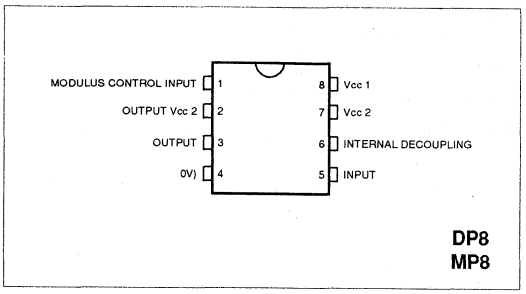


Figure 1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply Voltage 5.2V or 6.8V to 9.5V
- Power consumption: 26mW Typical

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. Junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2 max.	10V

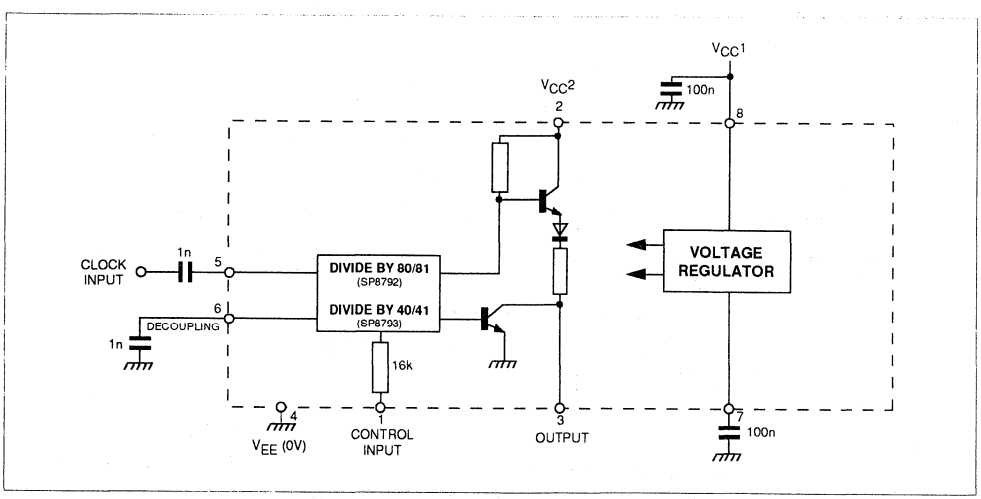


Figure 2 : Functional diagram SP8799

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):]

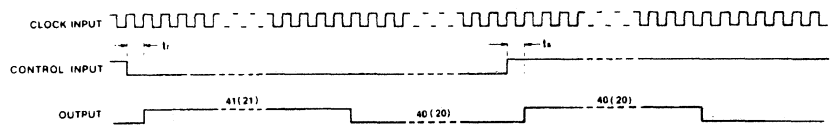
Supply voltage : Vcc = 5.2 ± 0.25V or 6.8V to 9.5V (see Operating Note 6): V_{EE} = 0V

Temperature T_{amb} = -40°C to +85°C

Characteristics	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input))	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked Vcc = 4.95V I_{OH} = 100µA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES

1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested onIt at 25°C



TRUTH TABLE FOR CONTROL INPUTS

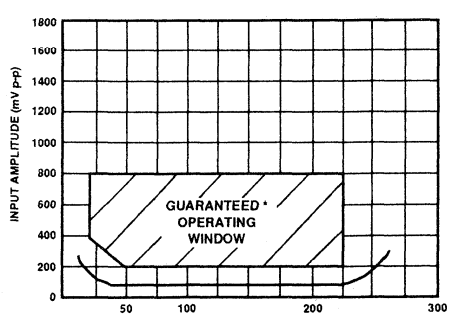
Control inputs	Division Ratio	
	SP8792	SP8793
0	81	41
1	80	40

Figure 3 : Timing diagramSP8792/3

NOTES

The set-up time ts is defined as the minimum time that can elapse between a L → H transition of the control input and the next L → H clock pulse transition to ensure ÷ 80 or 40 mode is selected.

The release time tr is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure ÷ 81 or 41 mode is selected.



*Tested as specified in table of Electrical Characteristics

Figure 4 : Input sensitivity SP8792/SP8793

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/~s is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

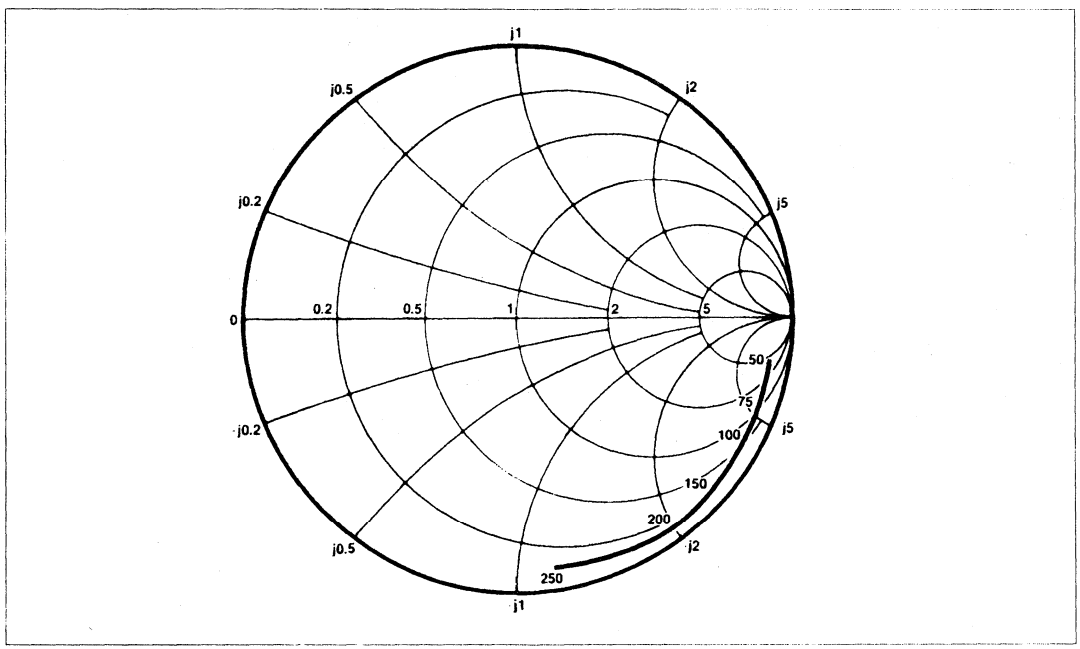


Figure 5 : Typical impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedance normalised to 50 ohms.

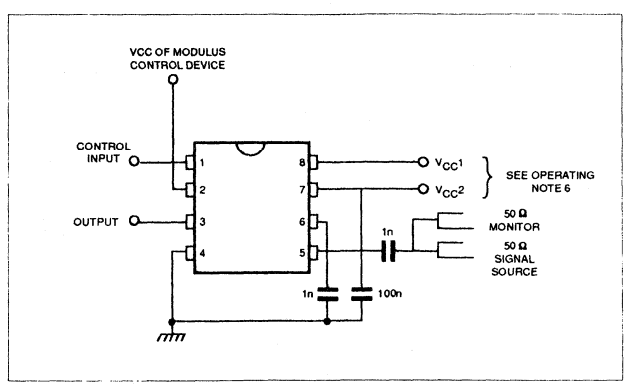


Figure 6 : Toggle frequency test circuit

SP8795

225MHz ÷ 32/33 TWO MODULUS DIVIDER

The SP8789 is a low power programmable ÷32/33 counter.It divides by 32, when the control input is in the high state and by 33 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

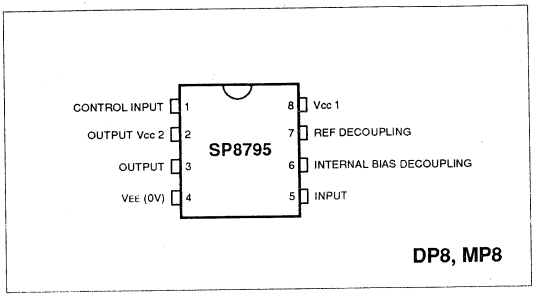


Figure 1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply Voltage 5.2V or 6.8V to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. Junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2	Max. 10V

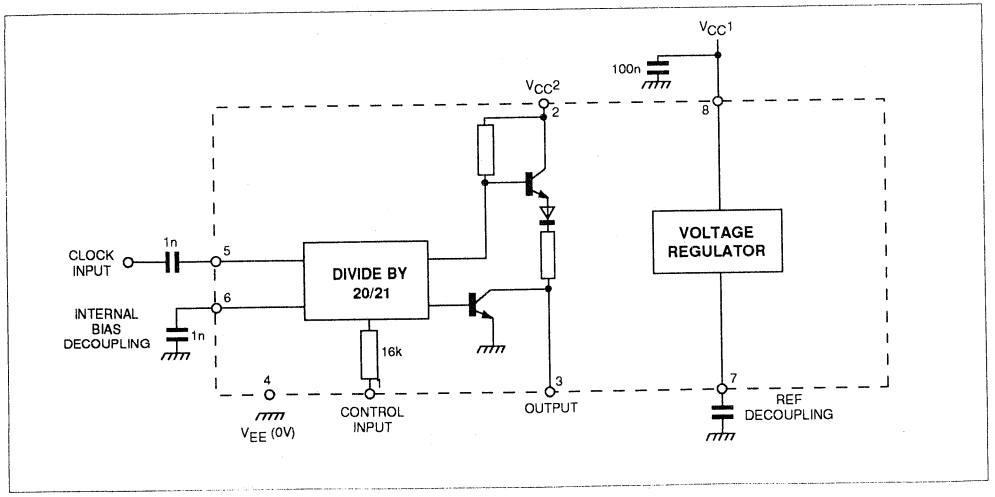


Figure 2 : Functional diagram SP8789

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):]

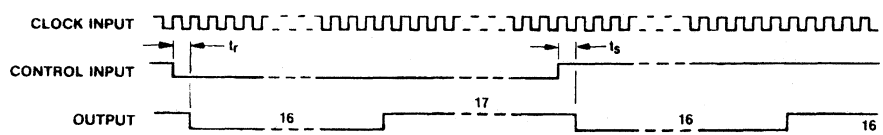
Supply voltage : Vcc 1 & 2 = 5.2 ± 0.25V or 6.8V to 9.5V (see Operating Note 7):

V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristics	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input))	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked Vcc = 4.95V I_{OH} = 100µA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES

1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested onlt at 25°C



TRUTH TABLE FOR CONTROL INPUTS

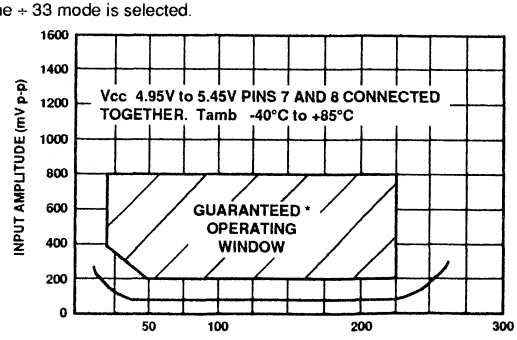
Control input	Division Ratio
0	33
1	32

Figure 3 : Timing diagramSP8785

NOTES

The set-up time ts is defined as the minimum time that can elapse between a L → H transition of the control input and the next L → H clock pulse transition to ensure that the ÷ 32 mode is selected.

The release time tr is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure that the ÷ 33 mode is selected.



*Tested as specified in table of Electrical Characteristics

Figure 4 : Input sensitivity SP8785

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/~s is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

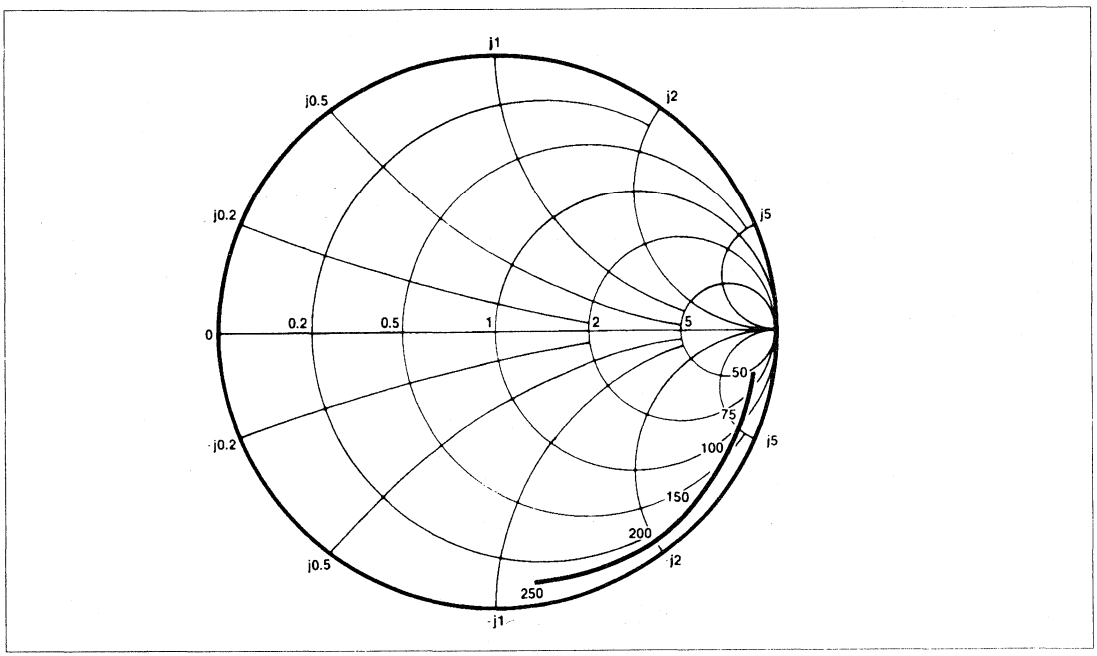


Figure 5 : Typical impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedance normalised to 50 ohms.

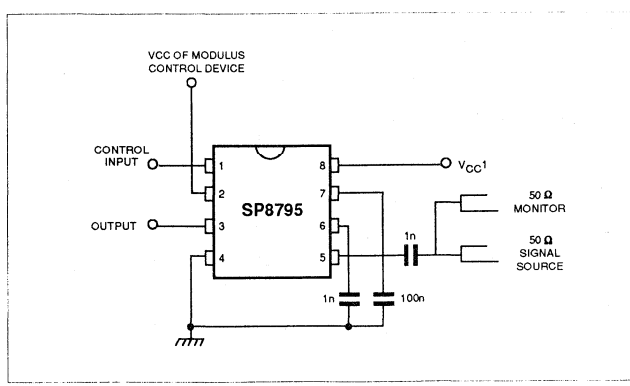


Figure 6 : Toggle frequency test circuit

DS 3296- 1

SP8799

225MHz ÷ 10/11 TWO MODULUS DIVIDER

The SP8799 is a low power programmable ÷10/11 counter. It divides by 10, when the control input is in the high state and by 11 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

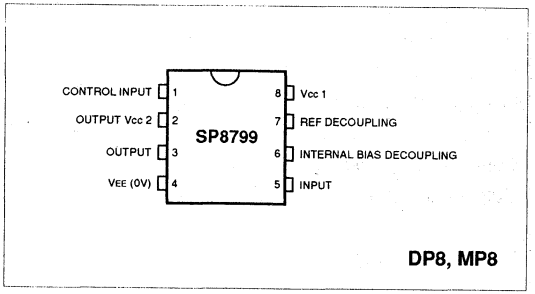


Figure 1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply Voltage 5.2V or 6.8V to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. Junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2	Max. 10V

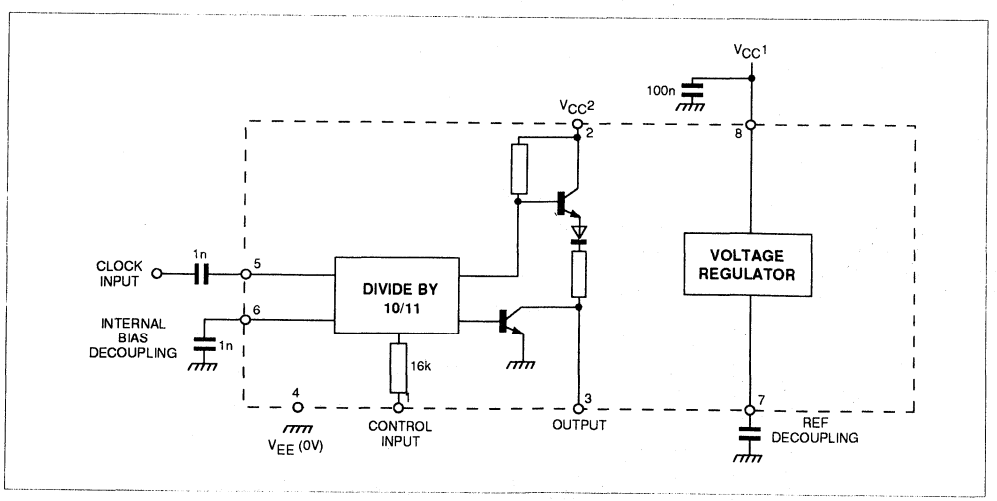


Figure 2 : Functional diagram SP8799

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):]

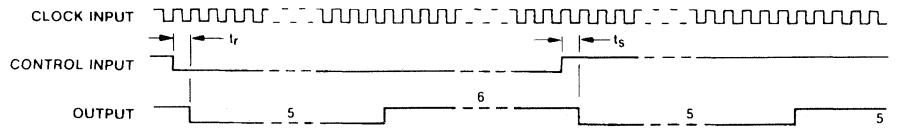
Supply voltage : Vcc 1 & 2 = 5.2 ± 0.25V or 6.8V to 9.5V (see Operating Note 7):

V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristics	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input))	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked Vcc = 4.95V I_{OH} = 100µA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES

1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested onlt at 25°C



TRUTH TABLE FOR CONTROL INPUTS

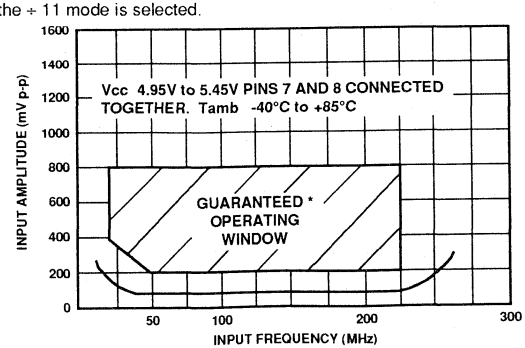
Control input	Division Ratio
0	11
1	10

Figure 3 : Timing diagramSP8799

NOTES

The set-up time ts is defined as the minimum time that can elapse between a L → H transition of the control input and the next L → H clock pulse transition to ensure that the ÷ 10 mode is selected.

The release time tr is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure that the ÷ 11 mode is selected.



*Tested as specified in table of Electrical Characteristics

Figure 4 : Input sensitivity SP8799

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/~s is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

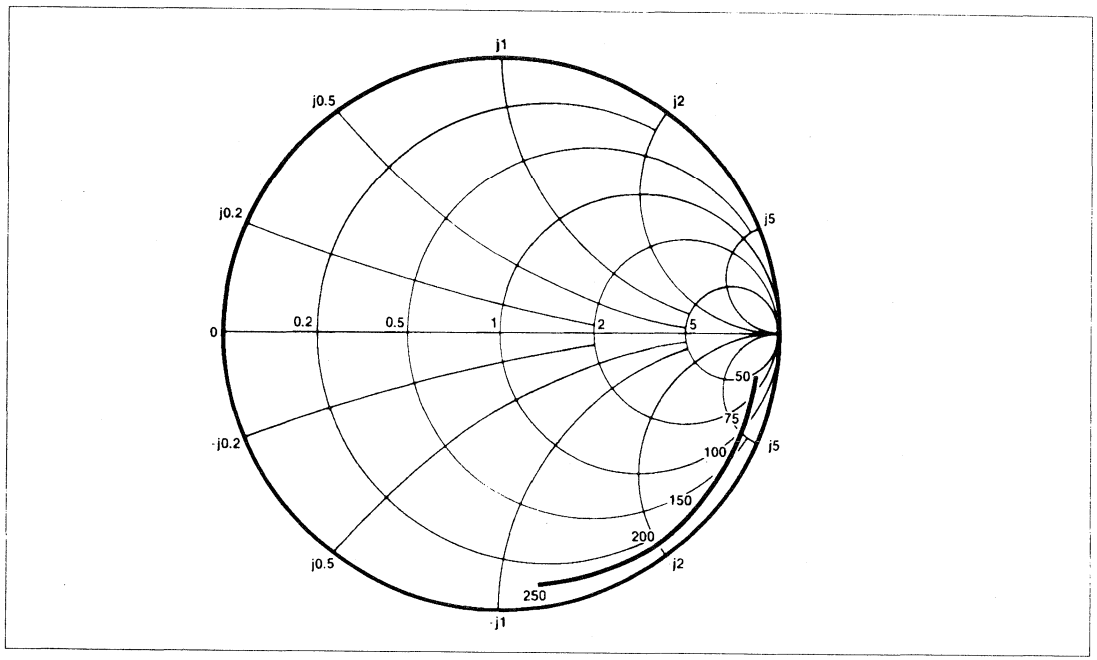


Figure 5 : Typical impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedance normalised to 50 ohms.

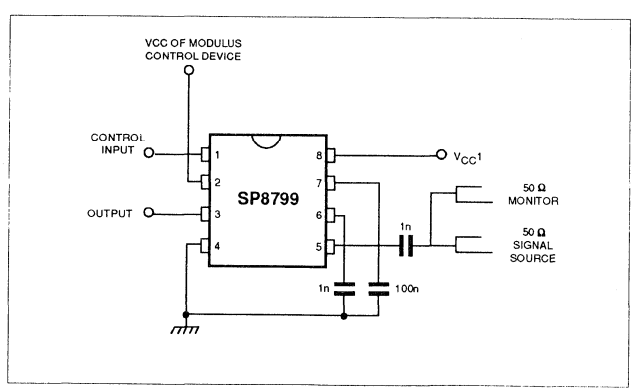


Figure 6 : Toggle frequency test circuit

Maintenance Data

Information for maintenance purposes only. Do not use for new designs.

NJ8820GG

FREQUENCY SYNTHESISER (PROM INTERFACE)

The NJ8820GG is a synthesiser circuit fabricated with the 2-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words in one of two modes. Data may be read from an external memory with the necessary timing signals generated internally.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

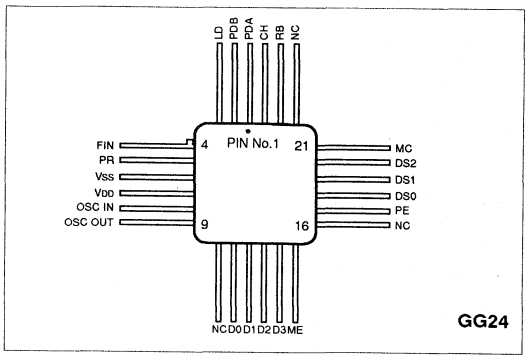


Fig. 1 Pin connections

FEATURES

- Low Power Consumption
- Direct Interface to ROM of PROM
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- > 10MHz Input Frequency

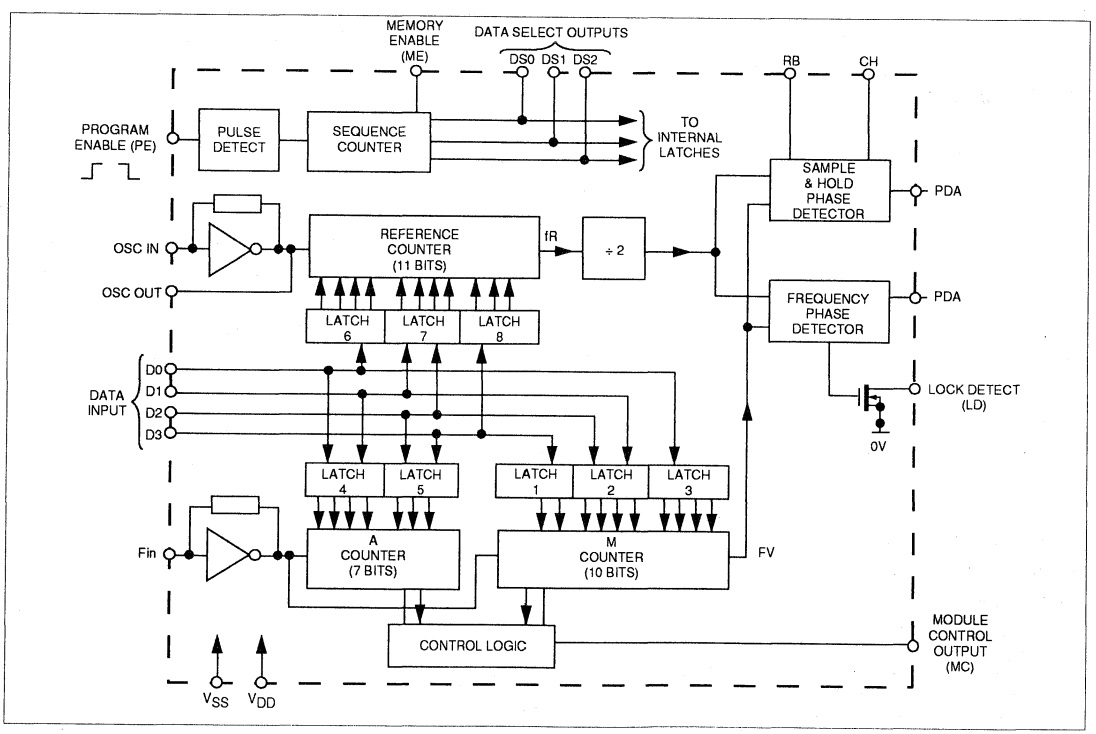


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD}-V_{SS} 5V ± 0.5V Temperature range -30°C to +70°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5.5	mA	
		0.7	1.5	mA	FOSC, FIN = 10MHz } 0 to 5V square wave FOSC, FIN = 1.0MHz }
OUTPUT LEVELS					
ME output					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
DS OUTPUTS					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 2mA
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low Level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	µA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input (PE)					
Trigger level	V_{bias} ±100mV			V	V_{bias} - self bias point of PE (nominally V_{DD}/2)

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	VDD = 5V, Input squarewave VDD-VSS Note 5
Propagation delay, clock to modulus control		30	50	ns	Note 2
Program enable pulse length, t_w	5			µS	Pulse to VSS or VDD
Data set-up time, t_{SI}	1			µS	
Data hold time, t_{HI}	10			ns	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.7
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	
Power supply rise time	100			µS	10% to 90% Note 4

NOTES

1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of samples switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. To ensure correct operation of power-on programming.
5. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. **Output at (V_{DD}-Vss)/2 when In lock**. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal . FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	PR	This pin allows selection between programming modes. For internal control the pin should be left open circuit and should be grounded to allow external control.
6	V_{SS}	Negative supply (normally ground)
7	V_{DD}	Positive supply
8,9	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
11,12,13,14	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
15	ME	An open-drain output for use in controlling the power supply to an external ROM or PROM. This output is low during the data read period and high impedance at other times.
17	PE	This pin has two functions. In internal mode a positive or negative pulse AC coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner. In external mode this pin is used as a strobe for the data. A logic high on this pin transfers data f rom the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
18,19,20	DS0-DS2	Internally generated three-state data select outputs which may be used to address external memory. In external mode these pins became inputs to control the addressing of data latches.
21	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.P +A where P and P +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control pre-scalers with a division ratio up to and including .128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ≥ A. Where every possible channel is required, the minimum division ratio should be P^2-P.
23	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and Vss
24	CH	An external hold capacitor should be connected between this pin and Vss.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}Vss): - 0.5V to 7V

Input voltage at any pin * V_{SS} -0.3V to V_{DD} +0.3V

Storage temperature: -65° C to +150° C

*Except on open drain outputs where this is 7V

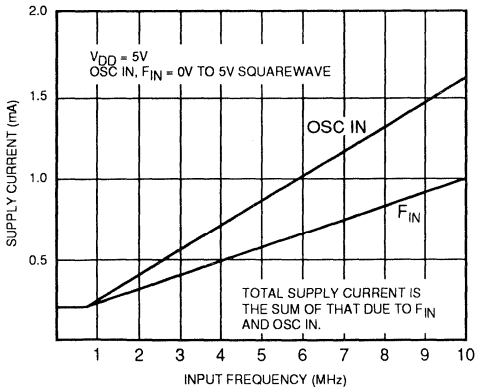


Fig. 3 Typical supply current versus input frequency

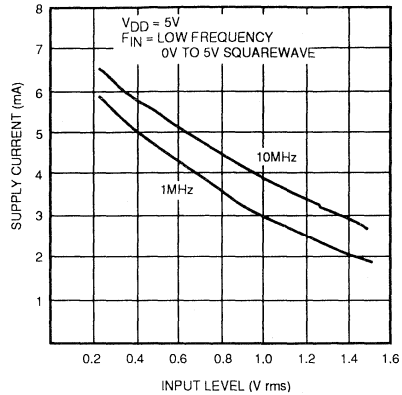


Fig. 4 Typical supply current versus input level, Osc In

PROGRAMMING IN INTERNAL MODE

This mode of operation allows program information to be obtained from an external ROM or PROM under control of the NJ8820GG. Twenty-eight data bits are required per channel arranged as eight 4-bit words leaving four redundant bits, two of which are available on the data bus driving the data-transfer time slot and may be used for external control porposes. A suitable PROM may be the 74S287 giving up to 32 channel capability. Note that the choice of PNP transistor and supply bypass capacitor on the ROM should be such that the ROM will power up in time: for example, at 10MHz oscillator frequency, the ROM must be powered up in less than 25µs.

Reading of this data is normally done in a single shot mode with the data read cycle started by either a positive or negative pulse on the program enable pin. The data read cycle is generated from a program clock at 1/64th of the reference oscillator frequency. A memory enable signal is supplied to allow power-down of the memory when not in use. Data select outputs remain in a high-impedance state when the program cycle is completed to allow the address bus to be used for other functions if desired.

Data is latched internally during the shaded portions of the program cycle and all data is transferred to the counters and latched during the data transfer time slot.

Alternatively, the PE pin may be grounded causing the data read cycle to repeat in a cyclic manner to allow continuous up-dating of the program information. In this mode external memory will be enabled continuously, (ME low) and the data read cycle will repeat every sixteen cycles of the internal program clock, i.e. every 1024/fosc seconds. This programming method is not recommended because of higher power consumption and the possibilities of noise injection into the loop from the digital data lines.

Power-on programming On power-up the data read cycle is automatically initiated making it unnecessary to provide a PE pulse on power-up. The circuit detects the power supply rising above a threshold point, (nominally 1 .5V) and after an internally generated delay to allow the supply to rise fully the circuit is programmed in the normal way. This delay is generated by counting reference oscillator pulses and is therefore dependent on the crystal used. The delay consists of 53248 reference oscillator cycles giving a delay of about 5ms at 10MHz.

To ensure correct operation of this function the power supply rise time should be less than 5ms, (at 10MHz) rising smoothly through the threshold point.

PROGRAMMING IN EXTERNAL MODE

The external mode of programming is selected by grounding the program pin, (PR). In this mode timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is as Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin lowwill disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.8.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig. 5 Data map

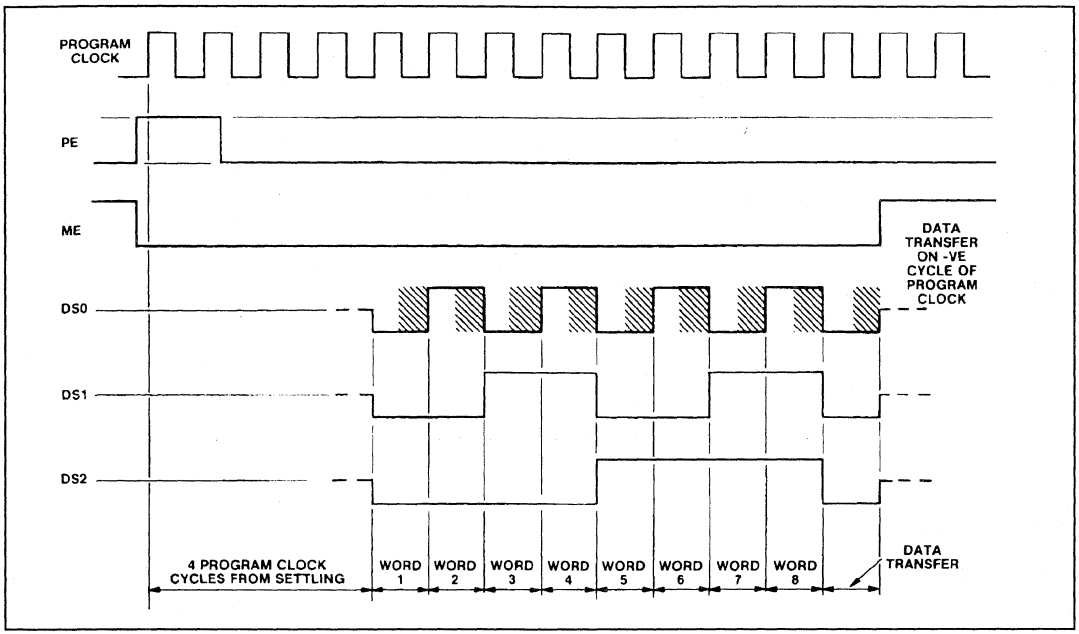


Fig. 6 Data selection

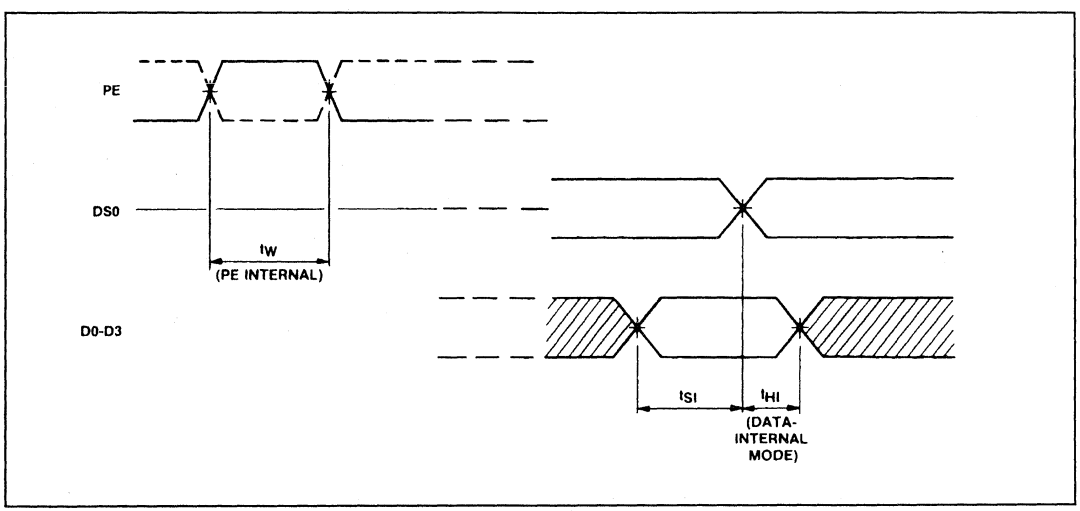


Fig. 7 Timing diagram

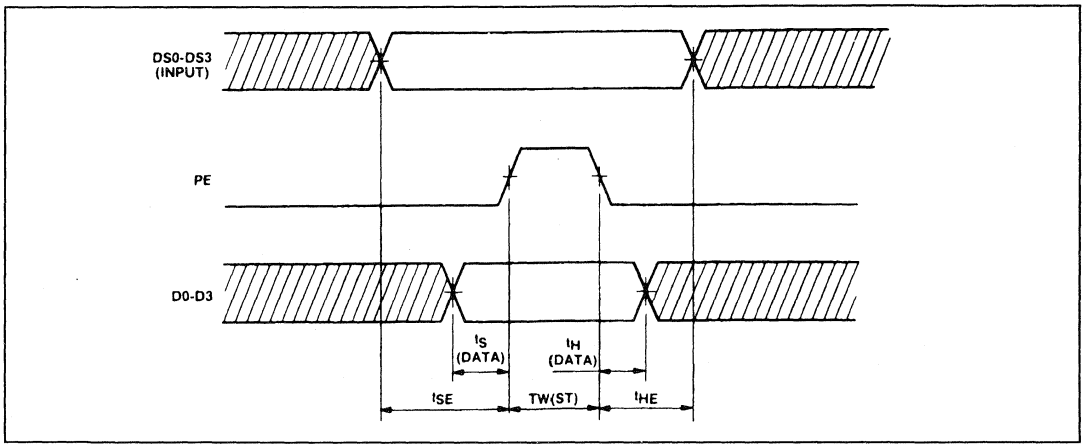


Fig. 8 Timing for external mode

PHASE COMPARATORS

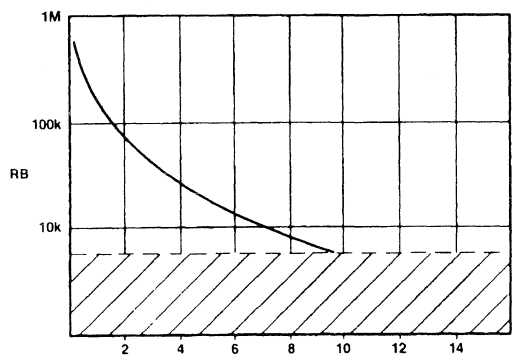
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phaselock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (V_{DD}-V_{SS})/2 and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically

$$\text{GAIN} = \frac{10\,[V_{DD}\text{-}V_{SS}\text{-}0.7\text{-}89(RB^{-1/2})]}{2 \times \pi\ 50 \times 10^{12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.9 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 89kn. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.9 shows the gain normalised to a 1 Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig. 9 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

NJ8821GG

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE)

The NJ8821GG is a synthesiser circuit fabricated with the 2-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words in one of two modes. Data may be read from an external memory with the necessary timing signals generated internally.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

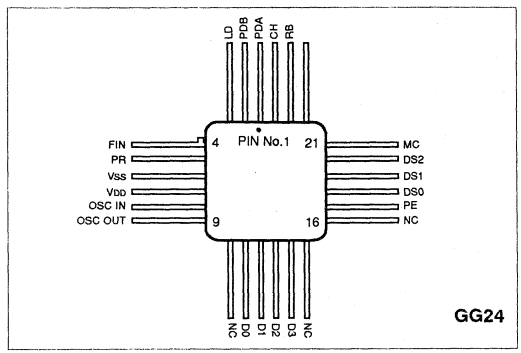


Fig. 1 Pin connections

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- > 10MHz Input Frequency

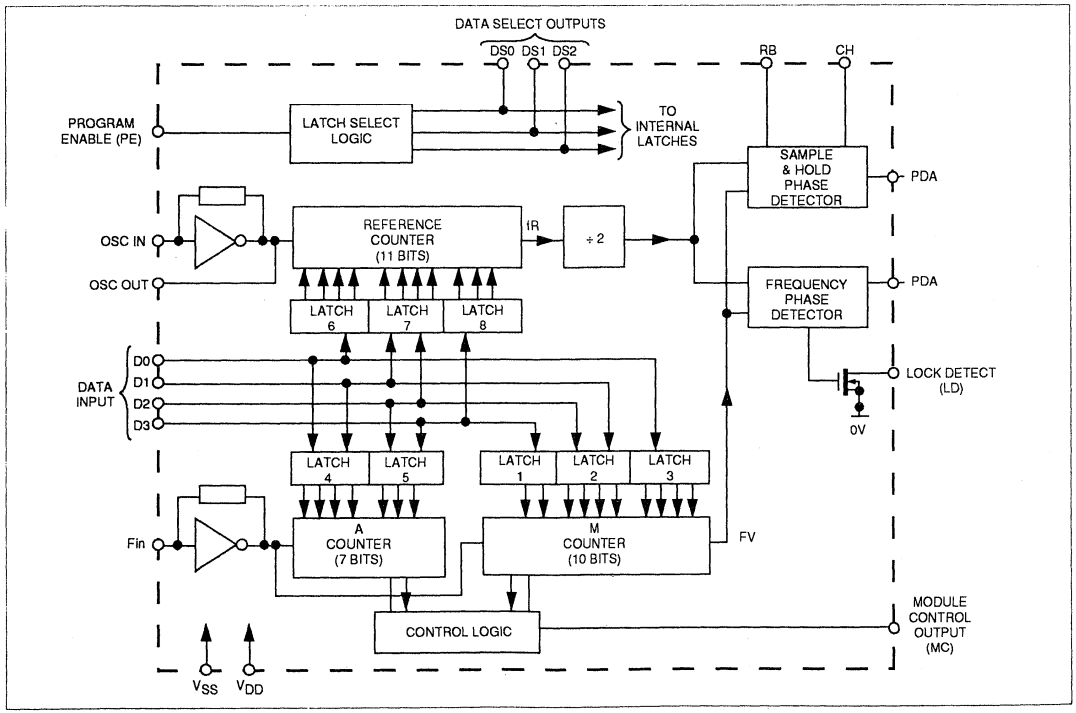


Fig. 2 Block diagram

NJ8821GG

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD}-V_{SS} 5V ± 0.5V

Temperature range -30°C to +70°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	7.0	mA	
		0.7	2.0	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
					FOSC, FIN = 1.0MHz }
MODULUS CONTROL OUT					
High level	4.6			V	source 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low Level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	µA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input (PE)					
High level	425			V	
Low level			0.75	V	
DS INPUTS					
High level	425			V	
Low level			0.75	V	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	VDD = 5V, Input squarewave VDD-VSS Note 5
Propagation delay, clock to modulus control		30	50	ns	Note 2
Strobe pulse width external mode, $t_{W(ST)}$	2			µS	
Data set-up time, $t_{S\,(DATA)}$	1			µS	
Data hold time, $t_{H\,(DATA)}$	1			µS	
Address set-up time, t_{SE}	1			µS	
Address hold time, t_{HE}	1			µS	
Digitail phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.6
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	

NOTES

1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of samples switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. To ensure correct operation of power-on programming.
5. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. **Output at (V_{DD}-Vss)/2 wilen In lock.** Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal . FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	PR	This pin allows selection between programming modes. For internal control the pin should be left open circuit and should be grounded to allow external control.
6	V_{SS}	Negative supply (normally ground)
7	V_{DD}	Positive supply
8,9	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
11,12,13,14	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
17	PE	This pin has two functions. In internal mode a positive or negative pulse AC coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner. In external mode this pin is used as a strobe for the data. A logic high on this pin transfers data f rom the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
18,19,20	DS0-DS2	Internally generated three-state data select outputs which may be used to address external memory. In external mode these pins became inputs to control the addressing of data !atches.
21	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.P +A where P and P +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including .128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ≥ A. Where every possible channel is required, the minimum division ratio should be P^2-P.
23	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and Vss
24	CH	An external hold capacitor should be connected between this pin and Vss.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD-VSS): -0.5V to 7V
Input voltage at any pin * V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature: -65°C to +150°C

* Except on open drain outputs where this is 7V.

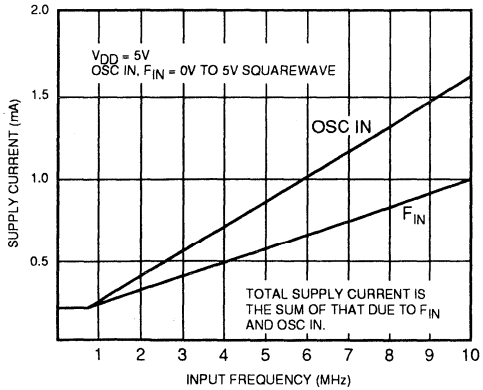


Fig. 3 Typical supply current versus input frequency

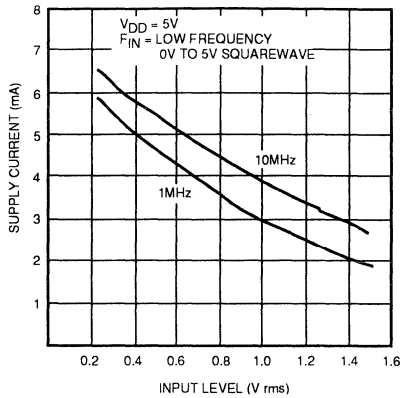


Fig. 4 Typical supply current versus input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.6.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig. 5 Data map

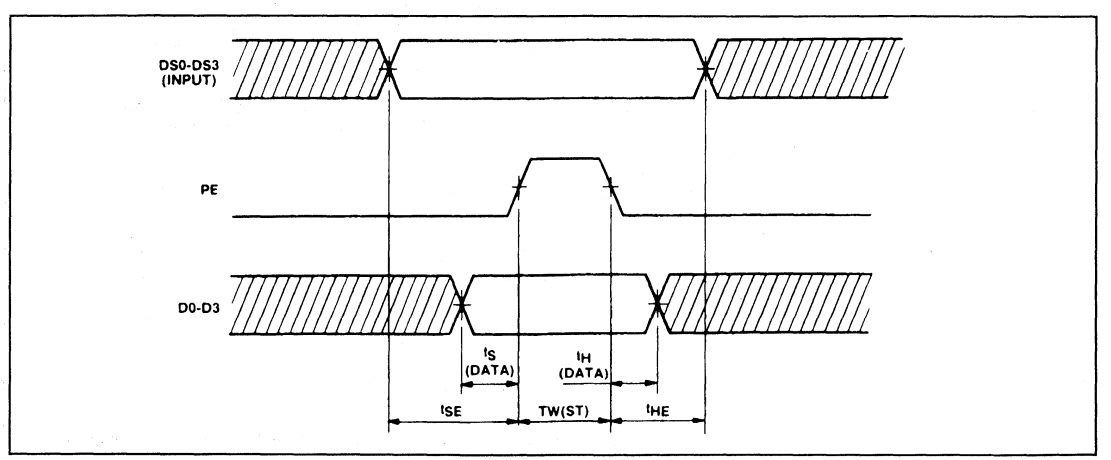


Fig. 8 Timing for external mode

PHASE COMPARATORS

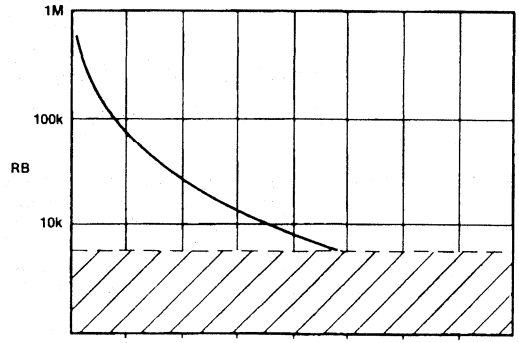
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phaselock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (VDD-VSS)/2 and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically

$$\text{GAIN} = \frac{10\,[V_{DD}\text{-}V_{SS}\text{-}0.7\text{-}89(RB^{-1/2})]}{2 \times \pi\, 50 \times 10^{12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.9 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 89kn. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.9 shows the gain normalised to a 1 Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig. 7RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

DS2469

SL6639-1

200MHz DIRECT CONVERSION FSK DATA RECEIVER

(NOTE. SL6639-1 is similar to SL6639 but with the beeper and LED driver omitted)

The SL6639-1 is a low power direct conversion radio receiver for the reception of frequency shift keyed transmissions. It features the capability of 'power down' for battery conservation.

The device also includes on chip adjustable channel filters, voltage references and a low battery flag indicator.

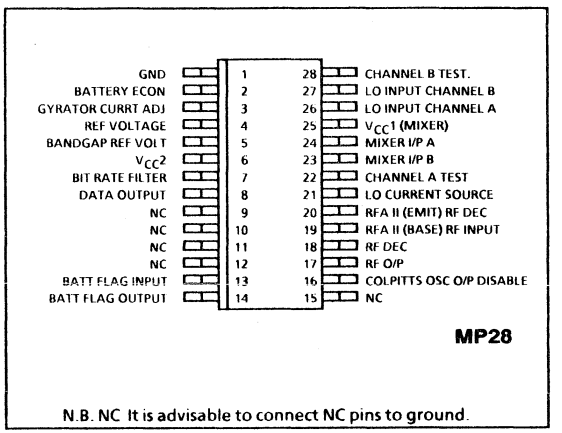


Fig.1 Pin connections - Top View

FEATURES

- Very Low Power Operation - typ. 3.7mW.
- Complete Radio Receiver in one Package.
- Operation up to 200MHz.
- 200nV Typical Sensitivity.
- Operates up to 1200 BPS.
- On Chip Tunable Active Filters.
- Minimum External Component Count
- Low Power Down Current Typical 5µA.
- Easy Alignment

APPLICATIONS

- Low Power Radio Data Receiver.
- Wrist/Watch Credit Card Pager.
- Radio Paging.
- Ultrasonic Direction Indication.
- Security Systems.
- Remote Control Systems

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	8V
Storage Temperature	-55°C to +150°C
Operating Temperature	-20°C to +60°C

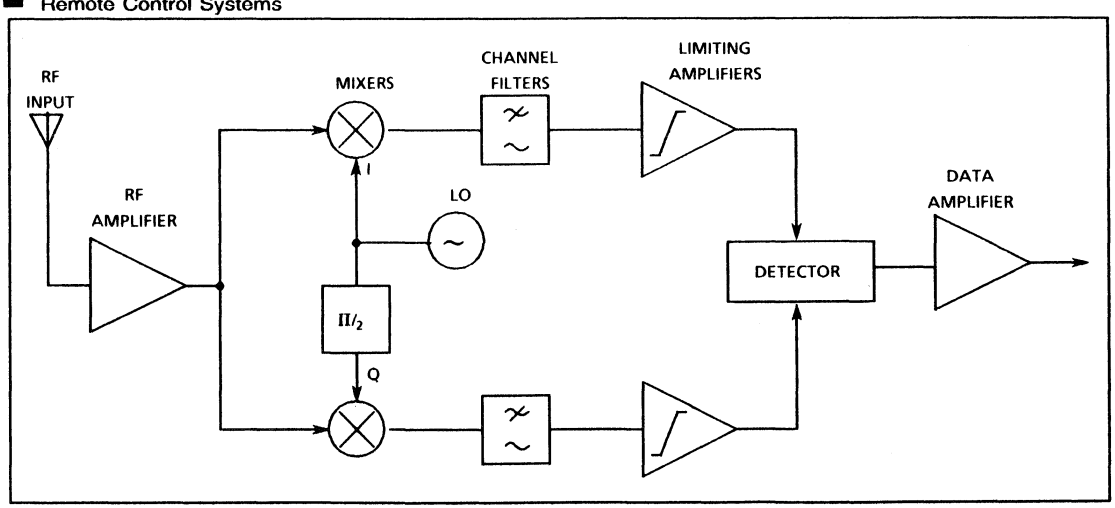


Fig.2 Block Diagram of SL6639-1 Direct Conversion Receiver

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 25°C, $V_{CC}1$ = 2.5V $V_{CC}2$ = 3.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Voltage V_{CC} 1	10, 25	0.9	1.3	2.8	V	$V_{CC}1 \leq (V_{CC}2) - 0.7$
Supply Voltage V_{CC} 2	6,16	1.8	2.3	3.5	V	
Supply Current I_{CC} 1	9,10,11,17 25,26,27		1.6	2.0	mA	(Beeper + LED) off. (IRF) Included
Supply Current I_{CC} 2	6,16		0.5	0.65	mA	(Beeper + LED) off
Power Down I_{CC} 1	9,10,11,17 21,25,26,27		5	12	µA	Batt Econ Low
Power Down I_{CC} 2	6,16		3	12	µA	Batt Econ Low
Bandgap Reference	5	1.15	1.22	1.35	V	
Voltage Reference	4	0.93	1.0	1.13	V	
RF Amplifier						
Supply Current (I_{RF})	17	510	580	650	µA	
Power Down	17				µA	Included in Power Down $I_{CC}1$
Noise Figure			5.5		dB	RS = 50Ω
Power Gain			14		dB	
Input Impedance	19					See Fig. 8
Mixers						
Gain to "IF" Test		33.5		40.5	dB	L.O. inputs driven in parallel with 50mV RMS @ 50MHz. IF = 2KHz
RF Input Impedance	23, 24					See Fig 9
LO Input Impedance	26, 27					See Fig 10
LO Drive Level	26, 27		10		mVrms	
LO DC Bias Voltage	26, 27				V	Equal to pin 25.
Oscillator						
Current Source	21	250	280	350	µA	
Power Down	21				µA	Included in Power Down $I_{CC}1$
Detector						
Output Current	7		±4		µA	
Decoder						
Sensitivity				70	µVrms	B.E.R. ≤ 1in 30 5KHz deviation @ 500 bits/sec BRF capacitor = 1nF
Output Mark Space Ratio	8	7:9		9:7		
Output Logic High	8	85			$\%V_{CC}2$	
Output Logic Low				15	$\%V_{CC}2$	

ELECTRICAL CHARACTERISTICS (Continued)

Test conditions (unless otherwise stated)
T_{amb} = 25°C, V_{CC} 1 = 2.5V V_{CC}2 = 3.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Battery Economy						
Input Logic High	2	(VCC2) -0.3			V	Powered Up
Input Logic Low	2			0.3	V	Powered Down
Input Current			0.05	1	µA	
Battery Flag						
Output High Level	14	85			%V_{CC}2	Battery Low
Output Low Level	14			15	%V_{CC}2	Battery High
Flag trig Level	13	V_R-25mV		V_R + 25mV	V	Voltage Reference (V_R) pin 4
Colpitts Oscillator						
Frequency	16		15		kHz	R = 330K, Pin 3 to GND
		15			kHz	R = 120K
				15	kHz	R = 360K
Output Voltage	16		20		mVp-p	RL ≫ 1MΩ N.B. Refer to Channel Filter Fig. 4.

RECEIVER CHARACTERISTICS (GPS Demonstration Board)

Test conditions (unless otherwise stated): Applications circuit diagram Fig.7; V_{CC}1 = 1.3V; V_{CC}2 = 2.3V; T_{amb} = 25°C, ; Collpitts oscillator frequency adjusted to 15kHz; mixer input A and B phase balance = 180°; local oscillator input A and B phase balance = 90°. Measurement methods as described by CEPT Res 2 specification.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Terminal Sensitivity Tone only 4/5 call reception			-124	-122	dBm	Δf = 4.5kHz, R_S = 50Ω, Fm = 256Hz
Deviation Acceptance			±2.5		kHz	3dB De-Sensitisation. $F_{IN} = F_{LO}$
Centre Frequency Acceptance		±2.5	±3		kHz	Δf = 4.5kHz fm = 256Hz (512Bps)
Adjacent Channel Rejection		65	70		dB	Δf = 4.5kHz Channel Spacing 25kKHz
Adjacent + 1 Channel Regection		65	70		dB	External capcitors on test
Third Order Intermod adj-1 + adj-2		52	53		dB	pins A and B.

PRINCIPLE OF OPERATION

The incoming signal is split into two parts and frequency converted to baseband. The two paths are produced in phase quadrature (see Fig 2) and detected in a phase detector which provides a digital output. The quadrature network may be in either the signal path or the local oscillator path.

The input to the system is an FSK data modulated signal with a modulation index of 18. This gives a spectrum as in Fig 3. f_1 and f_0 represent the 'steady state' frequencies (i.e. modulated with continuious '1' and '0' respectively). The spectrum in Fig 3 is for reversals (a 0-1-0-1-0-1 etc. pattern) at the system bit rate; f_c is the nominal carrier frequency).

When the LO is at the nominal carrier frequency, then a continuous '0' or '1' will produce an audio frequency, at the output of the mixers corresponding to the difference between f_0 and f_c or f_1 and f_c. If the LO is precisely at f_c, then the resultant output signal will be at the same frequency regardless of the data state; nevertheless, the relative phases of the two paths will reverse between '0' and '1' states. By applying the amplified outputs of the mixers to a phase discriminator, the digital data is reproduced.

TUNING THE CHANNEL FILTERS

The adjacent channel rejection performance of the SL6639-1 receiver is determined by the channel filters. To obtain optimum adjacent channel rejection, the channel filters' cut off frequency should be set to 8KHz. The process tolerences are such that the cut off frequency can not be accurately defined, hence the channel filters must be tuned.

Tuning is performed by adjusting the current in the gyrator circuits. This changes the values of the gyrator's equivalent inductance. The cut off frequency is tuned to 8KHz. To accurately define the cut off of the channel filters, a gyrator based Colpitts oscillator circuit has been included on the SL6639-1. The Colpitts oscillator and channel filters use the same type of architecture, hence there is a direct correlation between oscillator frequency and cut off frequency. By knowing the Colpitts oscillator frequency the channel filter cut off frequency can be estimated from Figure 4.

Once the channel filters have been tuned it may be necessary to disable the Colpitts oscillator. The Colpitts oscillator is disabled by connecting the Colpitts oscillator output/disable pin (pin # 16) to V_{CC} 2. This is needed since the Collpitts oscillator may impair the performance of the receiver.

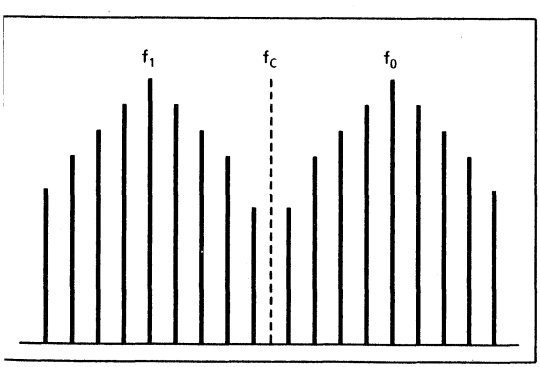


Fig. 3. Spectrum Diagram

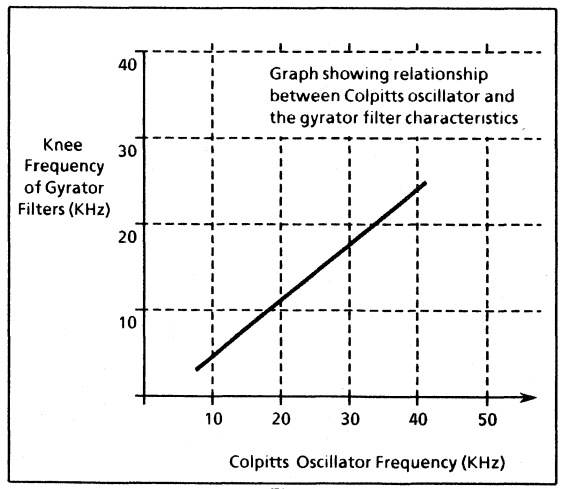


Fig. 4

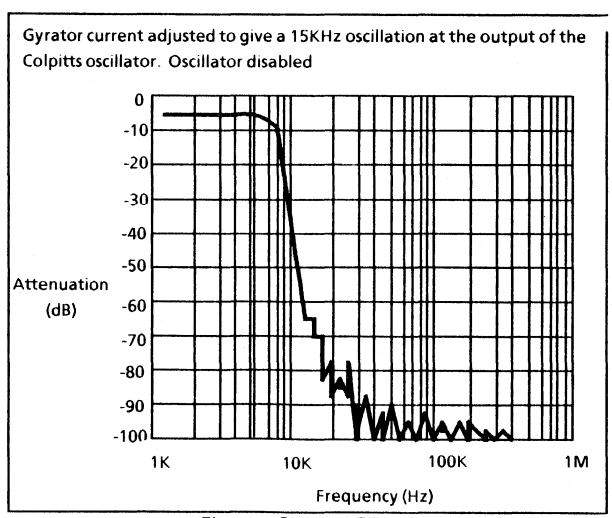


Fig. 5 Channel Filter Response

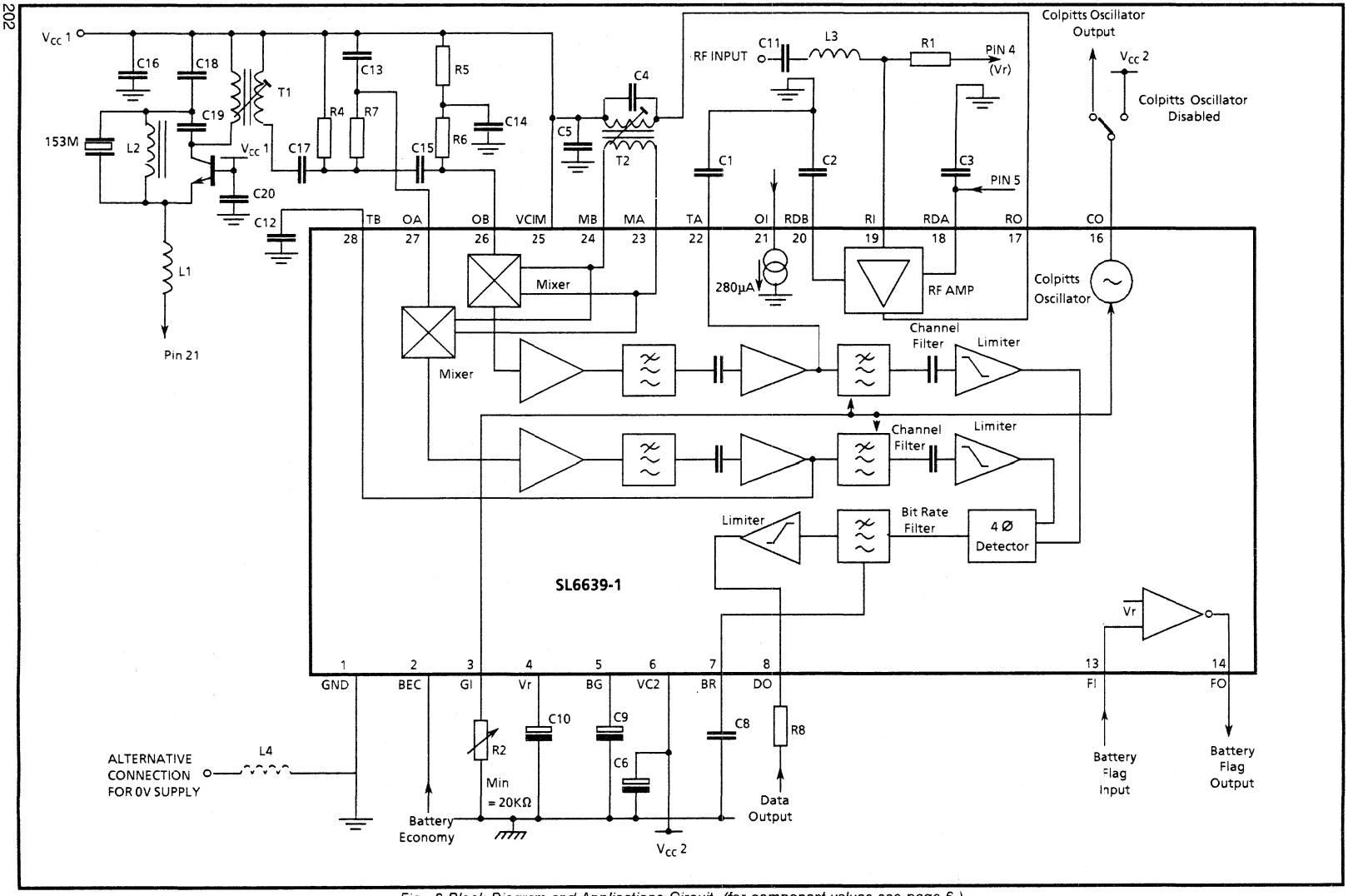


Fig. 6 Block Diagram and Applications Circuit (for component values see page 6)

COMPONENTS LIST FOR FIG.6

Capacitors	Resistors	Inductors	Transformers	Miscellaneous
C1 1nF C11 1nF C2 1nF C12 1nF C3 1nF C13 10nF C4 5.6pF C14 1nF C5 1nF C15 10pF C6 2.2µF C16 1nF C7 2.2µF C17 5.6pF C8 1nF C18 4.7pF C9 2.2µF C19 10pF C10 2.2µF C20 1nF	R1 2.2kΩ R2 500kΩ Variable R3 12kΩ R4 100Ω R5 100Ω R6 100Ω R7 100Ω R8 100KΩ	L1 10µH L2 220nH L3 150nH L4 10µH (optional)	T1 1:1 Transformer T2 Primary/Secondary Inductance = 200nH T3 Primary 3T, Secondary 4T	IC1 SL6639-1 TR1 SOT-23 Transistor with $f_t \geq 1.3$GHz (EG. ZETEX BFS 17) X1 153MHz 7th overtone crystal

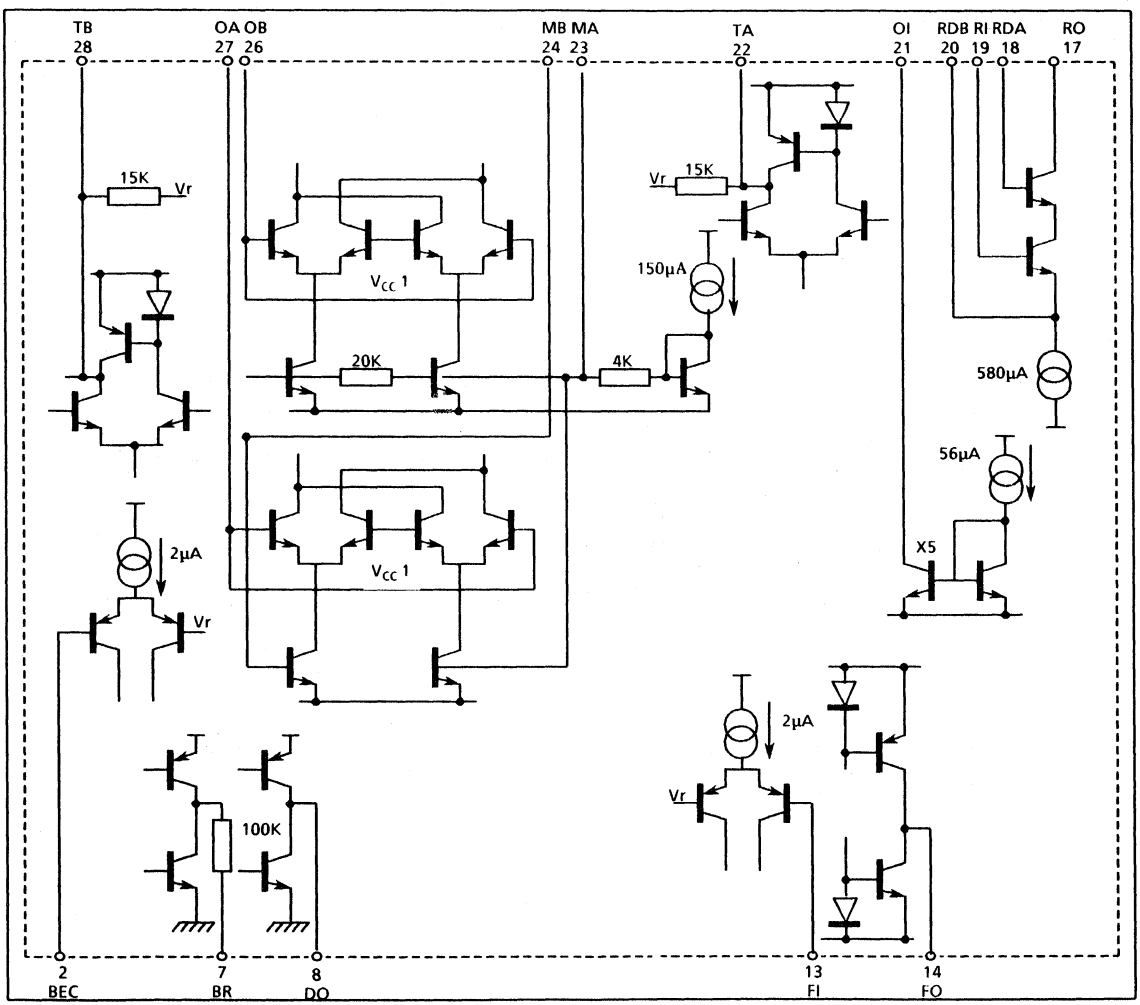


Fig. 7 Pinning Diagram of the SL6639-1

PIN	MNEMONIC	FUNCTION
1	GND	Ground
2	BEC	Battery Economy
3	GI	Gyrator Current Adjust
4	Vr	Reference Voltage
5	BG	Bandgap Reference Voltage
6	Vc2	V_{cc} 2
7	BR	Bit rate Filter
8	DO	Data Output
9		UNC or GND
10		UNC or GND
11		UNC or GND
12		UNC or GND
13	FI	Battery Flag Input
14	FO	Battery Flag Output

PIN	MNEMONIC	FUNCTION
15		UNC
16	CO	Colpitts Oscillator Output and Disable
17	RO	RFA I (collector) RF Output
18	RDA	RFA I (base) RF Decouple
19	RI	RFA II (base) RF Input
20	RDB	RFAII (emitter) RF Decouple
21	OI	LO Current Source
22	TA	Channel A Test
23	MA	Mixer I/P B
24	MB	Mixer I/P A
25	VCIM	V_{cc}1 (mixer)
26	OB	LO Input Channel A
27	OA	LO Input Channel B
28	TB	Channel B Test

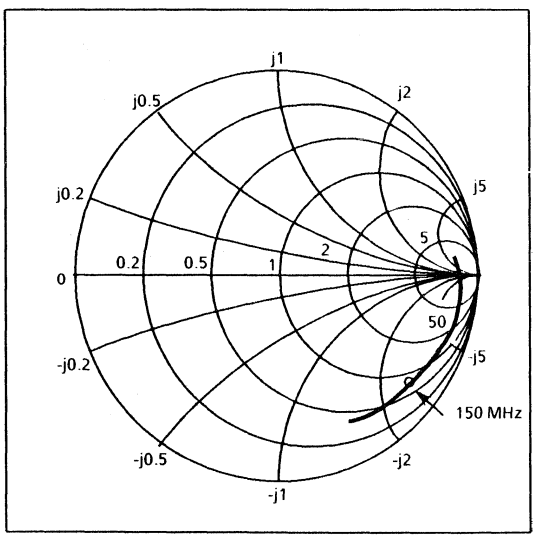


Fig. 8 Input Impedance S_{11} of SL6639-1 RF Amplifier (normalised to 50Ω)

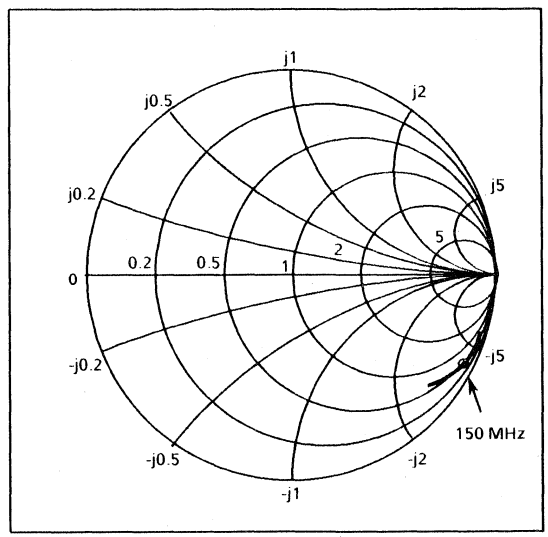


Fig. 9 Input Impedance S_{11} of SL6639-1 Mixer B i/p (pin23)

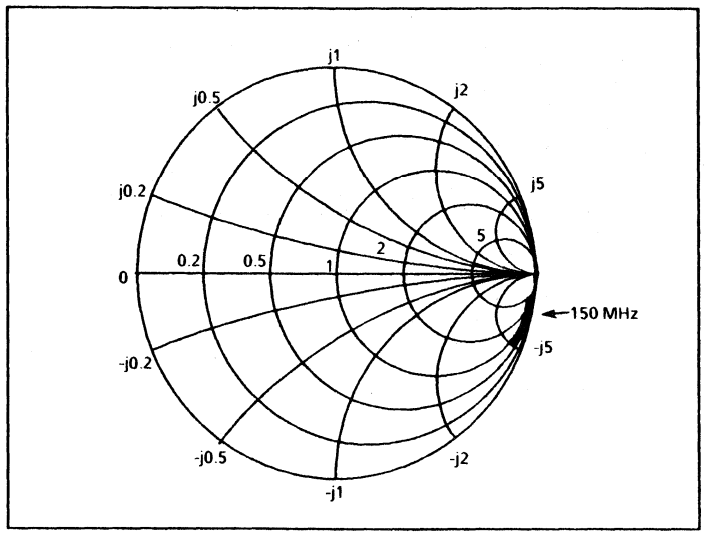


Fig. 10 Input Impedance S11 of SL6639-1 LO (i/p) (pin 26 or 27)

Power Supplies

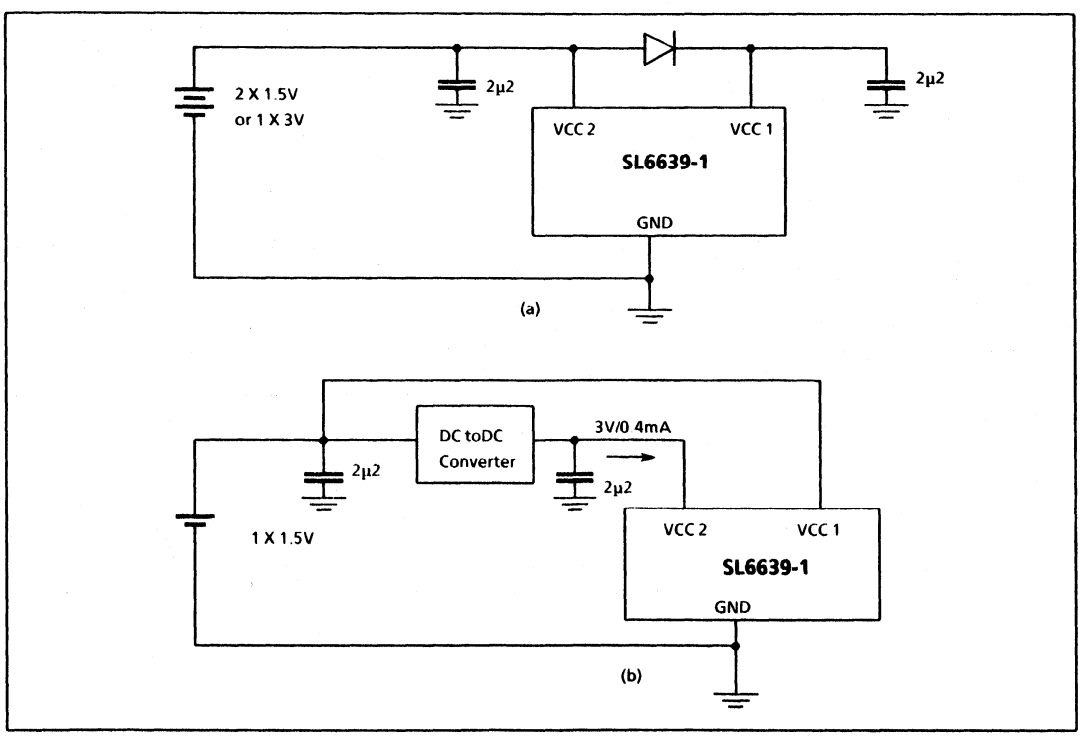


Fig. 13 (a) SL6639-1 Power Supply Options

METHOD FOR THE MEASUREMENT OF SENSITIVITY ON THE SL6639-1 RECEIVER

The method used by Plessey Semiconductors in the measurement of terminal sensitivity is essentially the same as that described in the Cept. Res2 Specification.

This method requires the following equipment:

1. A signal generator e.g. HP8640
2. A pocsag encoder
3. A pocsag decoder e.g. MV6639
4. An SL6639-1 Demo Board.
5. An interference free low impedance P.S.U. (Vcc1 and Vcc2 must be separate supplies and there must be at least 0.7V difference between them). Recommended supply configurations are shown in Fig. 13.

The test equipment and D.U.T. are set up as shown in Fig. 11.

The R.F. frequency is set to the nominal L.O. frequency of the receiver and the peak deviation is set to 4.5KHz.

Care must be taken to avoid long power supply leads and any ground loops. Any interference from the decoder will be reduced by the insertion of a high value resistor R1 (100KΩ)between the receiver data output and the decoder input.

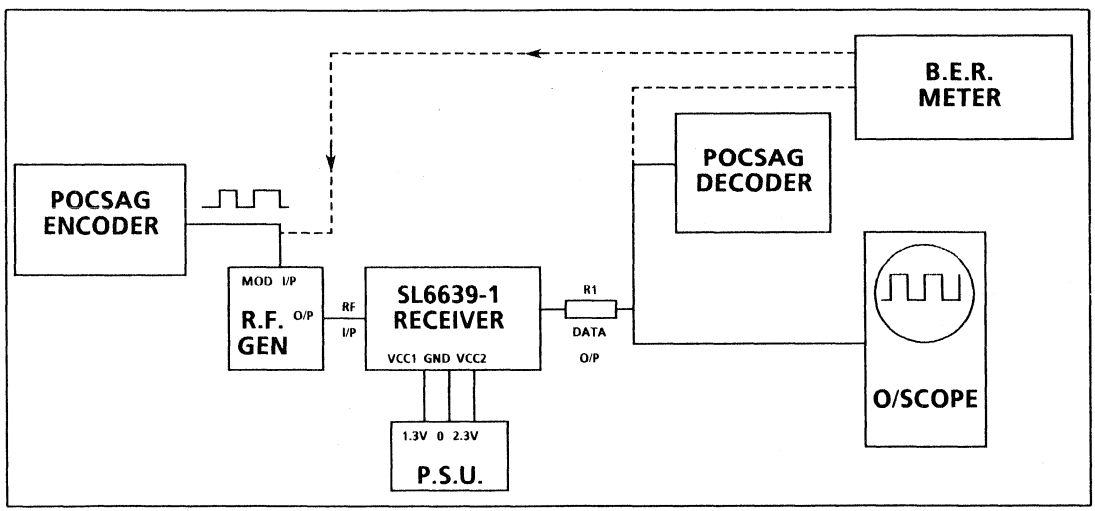


Fig. 11 Test System

The generator output level is reduced successively until the decoder responds just 4 out of 5 times to the encoder signal. This output level is then recorded as the sensitivity threshold of the receiver.

We find that this threshold correlates to a bit error rate of 1 in 30. The data output waveforms for an input level which produces a B.E.R. of 1 in 30 and for input levels 2dB above and below this level, are shown below (square wave input). It can be seen that the edge jitter increases dramatically at signal levels below the sensitivity threshold of -125dBm. Typical waveforms that can be seen on an oscilloscope around the sensitivity threshold level are shown in Fig. 12.

NB. In performing the sensitivity measurement great care should be taken in preventing coupling between test leads.

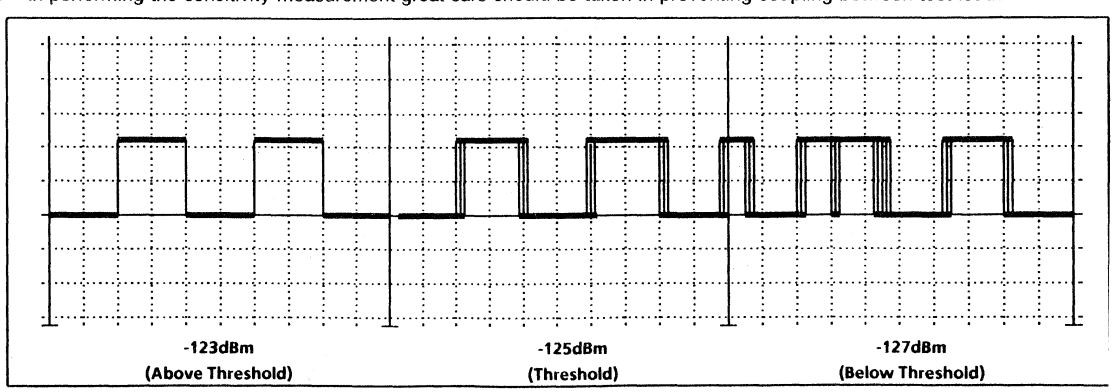


Fig. 12. Wave form at Data O/P

PAGER APPLICATION EXAMPLE

A typical 1 volt pager system suitable as a wrist watch application is shown in Fig. 13 (b). Only 3 integrated circuits are required to perform all the functions of a tone only pager. These are Plesseys SL6639-1 direct conversion radio receiver and the MV6639 POCSAG decoder plus a 1 volt E2PROM (eg Seiko Epson SPM28C51).

A 32KHz watch crystal is used as the reference frequency for the decoder. The resonator circuit for the tone outputs is similar to the crystal resonant circuit. The MV6639 performs all the function required for a POCSAG decoder for tone only and/or pager messaging at 512 or 1200 baud.

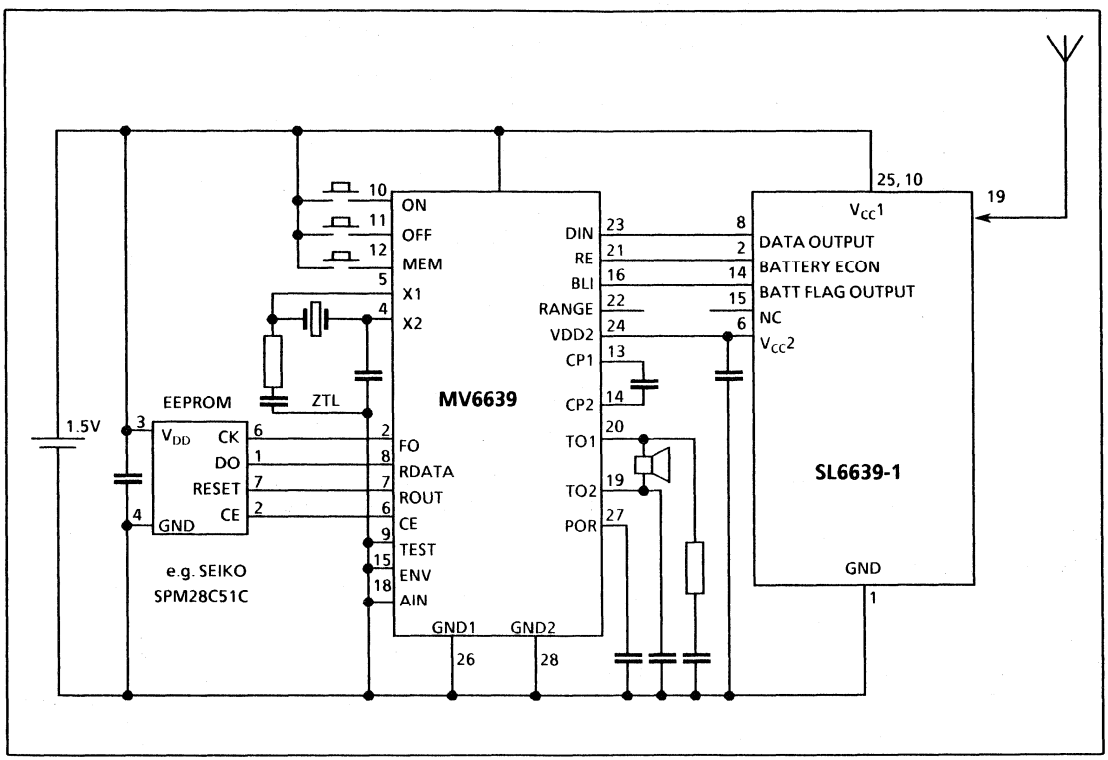


Fig. 13 (b) Application Example (Full Pager)

SL6639-1 DEMONSTRATION BOARD

This Application information describes a demonstration board using the SL6639-1 at 153MHz carrier with a data rate of 512bps. Modifications to the board for Applications at other frequencies and data rates are also described.

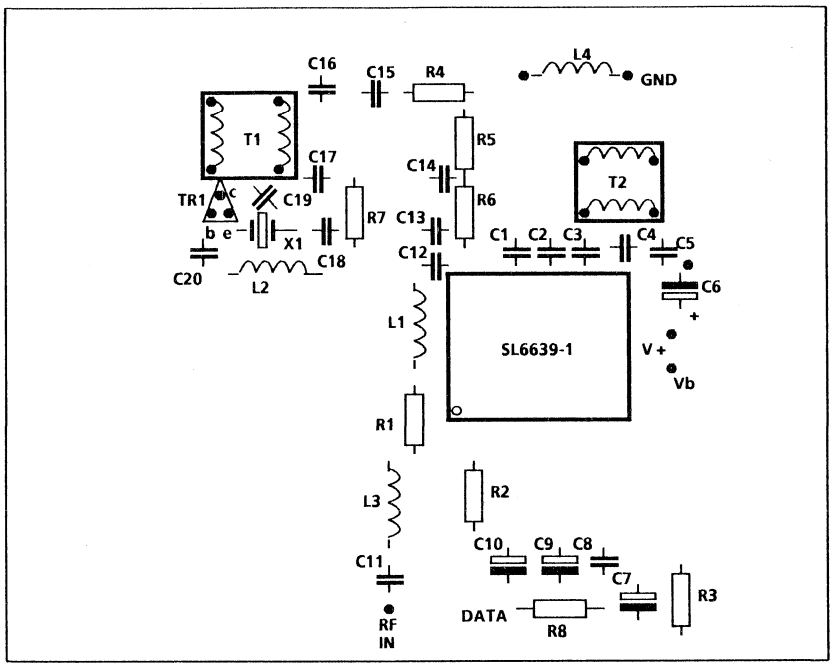


Fig. 14 Component Layout not to scale for reference purposes only

COMPONENT LIST FOR FIG. 14

Capacitors	Resistors	Inductors	Transformers	Miscellaneous
C1 1nF C2 1nF C3 1nF C4 2.2pF C5 1nF C6 2.2µF C7 2.2µF C8 1nF C9 2.2µF C10 2.2µF C11 1nF C12 1nF C13 10pF C14 1nF C15 10nF C16 1nF C17 4.7pF C18 1.5pF C19 5.6pF C20 1nF	R1 2.2KΩ R2 330KΩ * R3 12kΩ R4 100Ω R5 100Ω R6 100Ω R7 100Ω * Selected to give required filter cut off frequency	L1 10µH L2 220nH L3 150nH L4 10µH * * L4 can be replaced by a 100KΩ resistor.	T1 1.1 Transformer T2 Primary/Secondary Inductance = 200nH	IC1 SL6639-1 TR1 SOT-23 Transistor with $f_t \geq$ f1.3GHz (BFS 17) X1 153MHz 7th overtone crystal

OPERATION AT OTHER FREQUENCIES AND DATA RATES

The values given in the components list above are appropriate for frequencies nominally around around 153MHz. In order to use the receiver at other frequencies it is necessary to change the capacitors which are resonant with the transformers T1 and T2. These are C18 in series with C19 and C4 respectively. The ratio of C18 to C19 should be kept approximately the same as specified for 153MHz operation.

It is also necessary to change the values of capacitors C13 and C15 such that the reactance of these is equal to 100Ω at the required frequency.

It is of course necessary to use a crystal of the required frequency and stability. In order to use the receiver at higher data rates it is only necessary to reduce the value of C8, for example, at 1200bps, C8 = 470pf.

N.B. This PCB has been designed specifically to demonstrate terminal sensitivity. It is possible to connect an antenna to the board with suitable matching but no guarantee can be given regarding field strength sensitivity. However, with a suitably designed combination of PCB and antenna, a sensitivity of 5µV/M should be attainable.

Application Notes

Application Notes

AN94 - Using the NJ88C33 PLL Synthesiser - is a comprehensive 80 page application note on this product. AN112 - NJ88C24 Phase Detectors gives information on this product. Please contact your local GPS Customer Service Centre for copies of both these Application Nots.

154MHz Local Oscillator for the SL6649-1

AB38

Fig. 1 shows a 154MHz local oscillator circuit for the SL6649-1 FSK data receiver, using a 3rd overtone crystal which is series resonant at half the required output frequency.

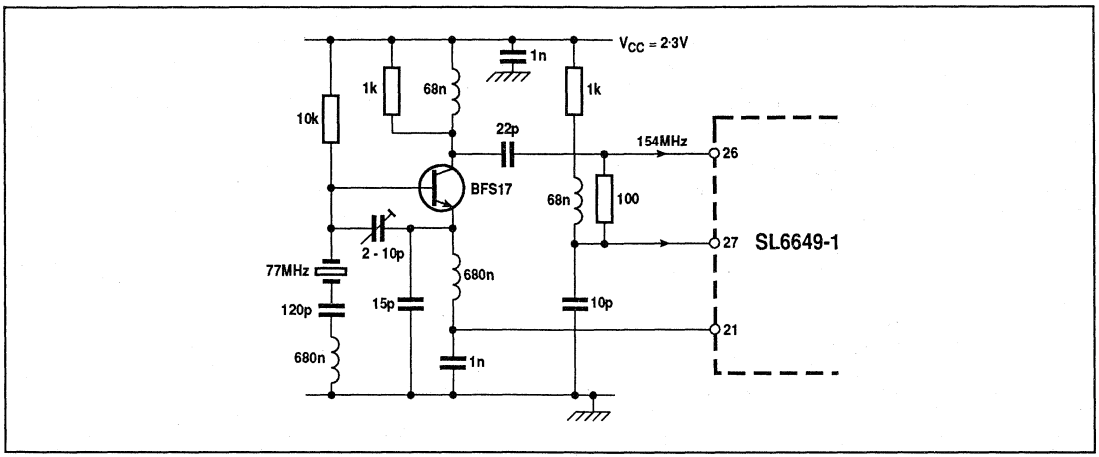


Fig. 1

Using the SL6649-1 at 230MHz

AB39

The SL6649-1 will operate at 230MHz using the internal LNA, although with reduced sensitivity. Suggested circuits for the LNA and local oscillator are shown in Figs. 1 and 2, respectively. X1 in Fig. 2 is a 3rd overtone series resonant crystal with a nominal frequency of one third the required LO frequency.

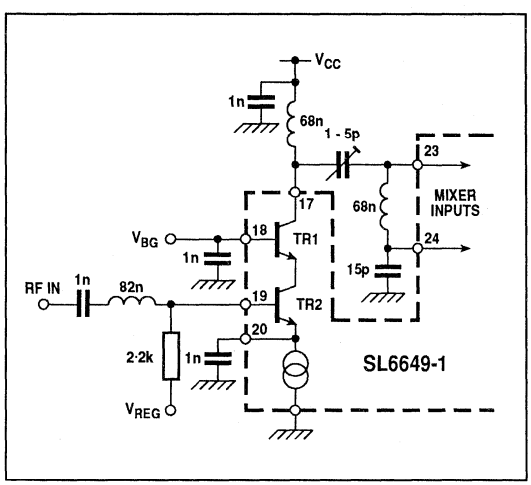


Fig. 1 230MHz LNA circuit

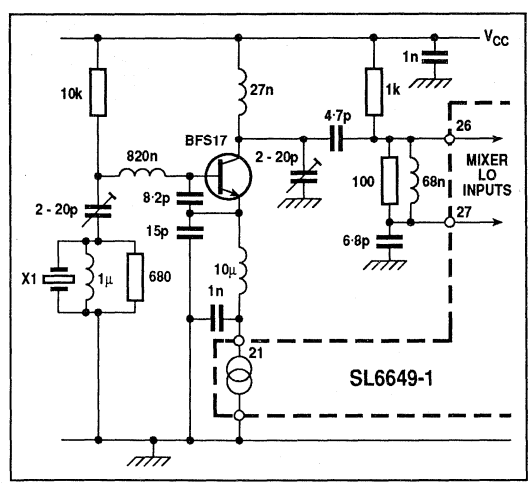


Fig. 2 230MHz local oscillator circuit

Tuned Amplifier Application for the SL6140 AN45

The SL6140 wideband AGC amplifier, when used in a 50Ω system, has a gain of 15dB. By tuning, or matching, the inputs and outputs of the device the gain can be increased. This produces a higher gain amplifier that will work over a limited bandwidth. The bandwidth of the amplifier depends upon the Q factor of the tuned/matching circuits used.

Fig. 1 shows a single ended amplifier with tuned input and output networks.

The input circuit consists of a parallel LC network connected across the differential inputs. The input signal is applied to one input, via a coupling capacitor (C1), the other input being decoupled. The coupling capacitor also forms part of the impedance matching network, matching a 50Ω source with the high impedance of the device (see Smith chart, Fig. 3). The tuned frequency is given by the following equation:

$$f = \frac{1}{2\pi \frac{\sqrt{L \times C \times C1}}{\sqrt{(C + C1)}}}$$

The output circuit consists of a parallel LC network connected from one of the open collector ouputs of the device to V_{CC}. The coupling capacitor (C2) and LC network transforms the 50Ω load to a high impedance load for the open collector outputs of the device, hence improving the gain.

By adjusting C1 and C2 the gain can be optimised, but if too high an impedance is seen by the input or output of the device the circuit may oscillate. L1 and L2 are adjusted to set the tuned frequency.

The high gain is achieved at the expense of bandwidth, so for maximum gain the matching network should be designed to provide the minimum bandwidth necessary for the particular application.

An alternative method of tuning the output of the device is to transformer-couple to the 50Ω load as shown in Fig. 2. The primary winding is connected across the outputs (a centre tap providing V_{CC}) and resonated at the required frequency with a capacitor. This circuit has a 6dB improvement of gain over the previous circuit as both outputs are used.

PCB LAYOUT

For best performance a ground plane should be used with 50Ω source and load. Also the matching network and decoupling capacitors should be placed as close to the device as possible.

If a very high gain, low bandwidth amplifier is required the addition of some shielding between input and output may be necessary to prevent oscillation.

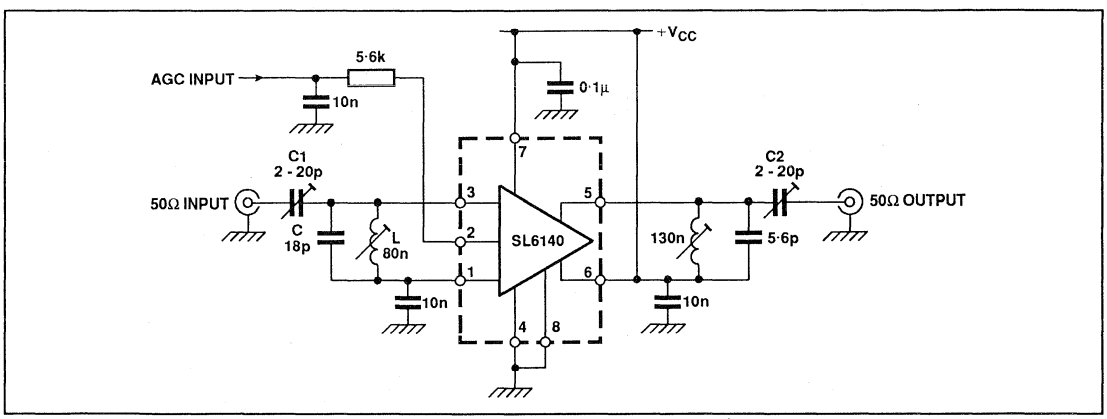


Fig. 1 A 100MHz tuned amplifier application with 35dB power gain (CM pinout)

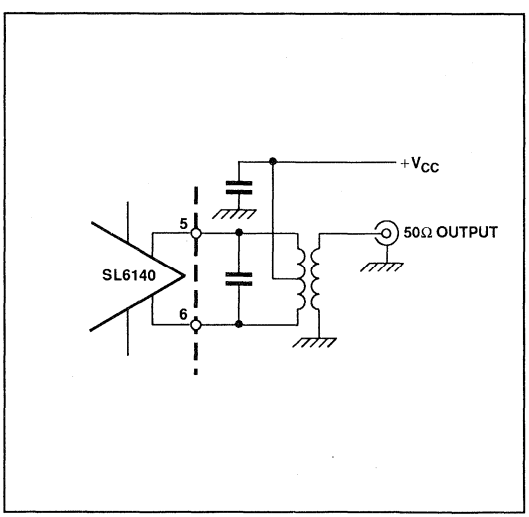


Fig. 2 Differential tuned output

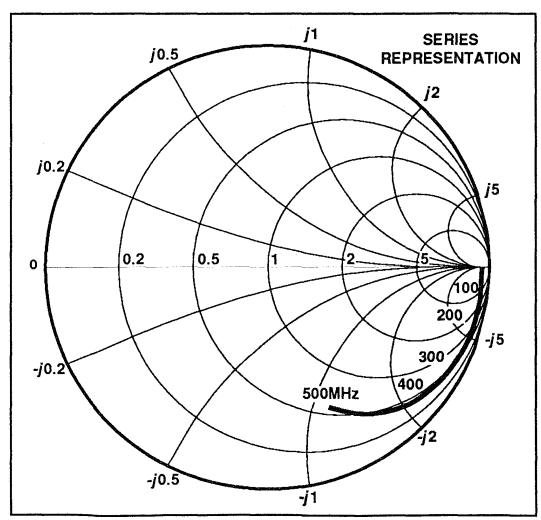


Fig. 3 Input impedance of SL6140 (50Ω normalised)

A FREQUENCY SCANNING SYSTEM FOR THE SL6639-1

This applications note describes the circuits required to scan the local oscillator of the SL6639-1 detect a transmission and received data before moving on to scan the remainder of the frequency band. No expensive circuitry has been employed and apart from the local oscillator the circuits run at audio frequencies.

The circuits shown can be connected to the standard SL6639-1 applications board with long leads as no RF frequencies are involved.

Only minor modification of the local oscillator on the demonstration board is required. This entails removing the crystal and adding a voltage controlled varicap diode to tune the local oscillator over the required band. The local oscillator is of the Colpitts type.

FEATURES

- Low Additional Cost
- Low Frequency Circuits
- Adjustments for Word length, sweep rate, and sweep range provided.

PRINCIPLE OF OPERATION

The local oscillator is scanned through the required band by the ramp generator shown in figure 3. When a signal appears within this band the stop circuit shown in figure 2 generates a series of stop pulses which are detected and used to slow down the ramping voltage. Hence the local oscillator moves through the received signal at a slow rate giving the SL6639-1 time to output the required number of data bits.

The stop signal is generated as the local oscillator reaches a frequency which is 1kHz before the first FSK side band. Therefore with the standard ±4.5kHz deviation stop pulses will be generated as the local oscillator reaches -5.5kHz from the centre of the received signal. Stop pulses will also be generated at +5.5kHz for systems which scan the band in both directions.

The stop signal can also be used with P2 in Fig.3 removed, the circuit will then stop sweeping at 5.5kHz before the centre of the band. A DC voltage could then be added to the Veractor voltage to step the local oscillator into the centre of the band.

THE STOP CIRCUIT FIG 2.

This circuit consists of a high impedance amplifier followed by a gyrator circuit which is then followed by a comparator. The circuits are best implemented using the Plessey TAB 1043 Quad OP-amp.

The signal from pin 28 of the SL6639-1 is amplified and fed to an LC tuned circuit with a resonant frequency of 1kHz. The inductor in this tuned circuit is 1Henry and therefore best implemented using two OP-amps configured as a gyrator. When the LC tuned circuit resonates at an amplitude above a threshold set on the comparator the stop pulses are produced.

THE RAMP CIRCUIT FIG 3.

The ramp circuit has been designed using a constant current source (D2 and T3) feeding into a capacitor. When the ramp reaches a threshold set by P3, It is reset by switching on T4. The stop pulses from the stop circuit are peak detected by D1 and when this peak voltage reaches 1.4V T1 switches on, this in turn switches T2 off. When T2 is switched off the current feeding the ramp capacitor is drastically reduced therefore the ramp down and the LO sweeps through the signal at a slow rate (set by P2). The SL6639-1 will then output the required data.

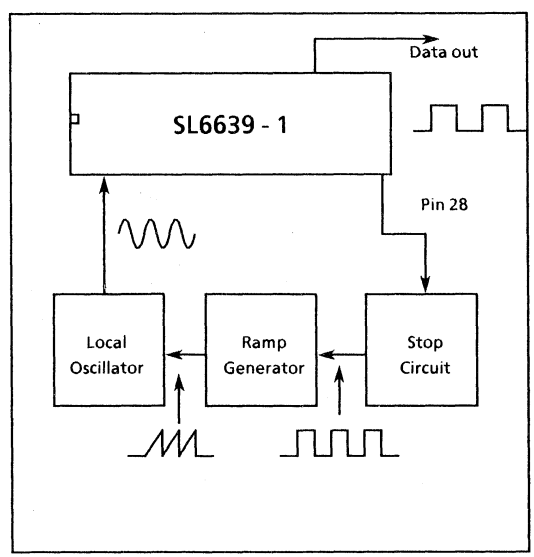


Fig.1 Block diagram

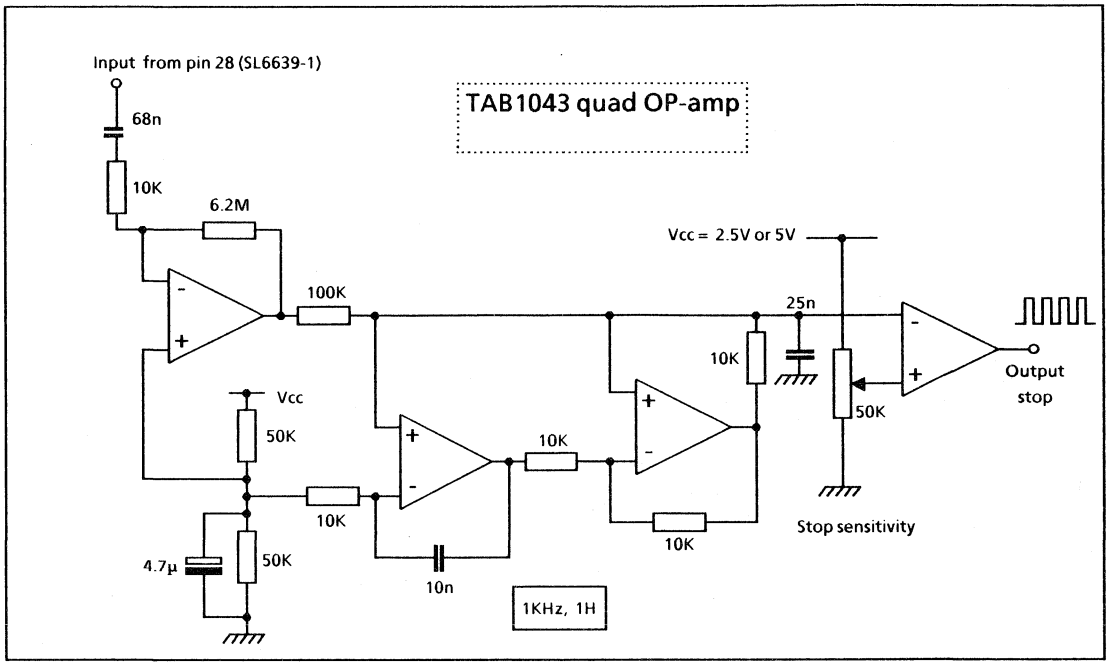


Fig 2 Gyrator Stop circuit

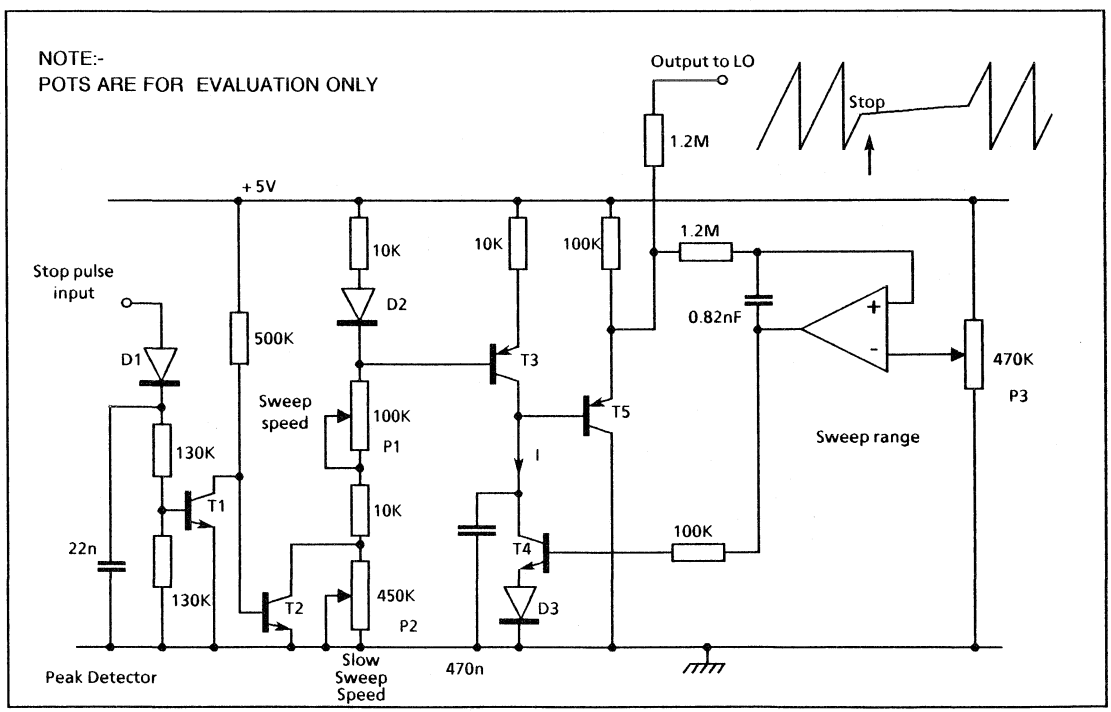


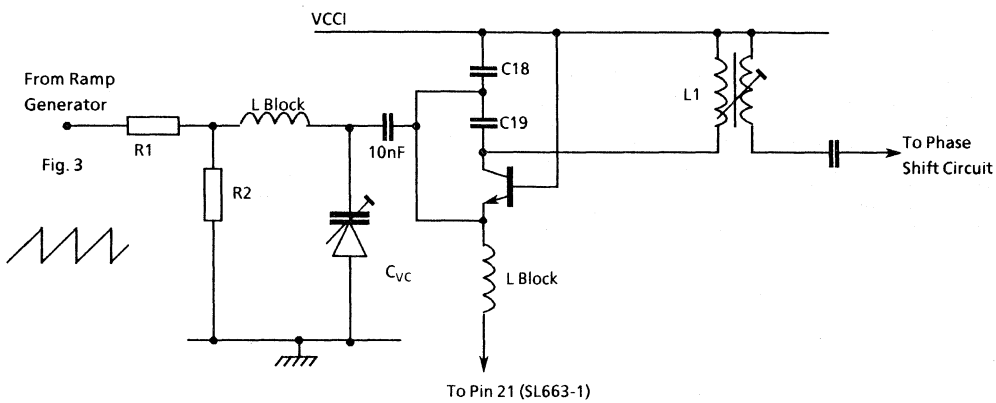
Fig 3 Ramp Generator

LOCAL OSCILLATOR

The local oscillator for the sweep system can be implemented using a Colpits oscillator and a VARACTOR diode. The ramp voltage is fed from the ramp generator to the varicap diode and therefore its capacitance changes, this in turn changes the frequency of the tuned circuit and hence its frequency will ramp over a small frequency range.

Example of.

L.O. using SL6639 Oscillator with XTL Removed.



R1 and R2 are chosen for desired frequency and sweep range.

Varactor Diode Capacitance Appears in Parallel with C18.

$$fc = \frac{1}{2\pi} \sqrt{\frac{1}{L1\left[\frac{(Cvc + C18) \times C19}{(Cvc + C18) + C19}\right]}}$$

The component values depend upon the choice of centre frequency and sweep range required.

USING THE SL6639-1 AT 500MHz

This Application Note describes an external amplifier which will allow the Plessey SL6639-1 single chip FSK radio receiver to be used within the range of 350MHz to 500MHz.

The SL6639-1 specification states that the maximum operating frequency of the device is 200MHz. The reason for this limit is that the device has been optimised mainly for paging receivers at 153MHz, and hence the relatively power hungry input amplifier has been designed for minimum power consumption at 200MHz. This means that the input amplifier response soon rolls off after 200MHz.

The frequency response of the two mixers on board the SL6639-1 is much wider than the input amplifier. Measurements have shown that the response of these low power mixers is virtually flat up to 500MHz, hence the addition of an external wideband amplifier will allow the device to be used for Industrial telemetry at 458.5 to 458.8MHz, car theft alarms at 458.9MHz, (Fig 2), fixed alarms at 458.8250MHz, transportable and mobile alarms at 458.8375MHz plus many other security and paging systems at high frequency.

FEATURES

- Very Wide Dynamic Range +15dBm to -123dBm at input Terminal
- Low Power <3mA Total (SL6639 + External Amp.)
- High Terminal Sensitivity of 200nV
- Single 3V Supply
- Alignment can be performed using 1MHz Scope on
- Pin 28
- Low Additional Cost
- Small Antenna due to High Frequency

SL6639 INTERNAL AMPLIFIER

The amplifier included within the SL6639-1 is a standard cascode pair, ie one transistor configured as a common emitter amplifier with another transistor used in common base configuration in its collector. Cascode amplifiers are widely used as they give high input impedance and gain at high frequencies. This is due to reduced Miller capacitance as the collector of the common emitter configured transistor is at a fixed voltage, hence negative feedback to the input will be reduced.

The SL6639-1 has yet another trick up its sleeve. To improve the receiver dynamic range, the input amplifier is powered down if the input signal exceeds about -30dBm. This is achieved by using an on chip AM detector prior to the mixers. This AM detector is connected to the current source which powers the input amplifier. Switching this current source off prevents mixer overload in all practical applications,.

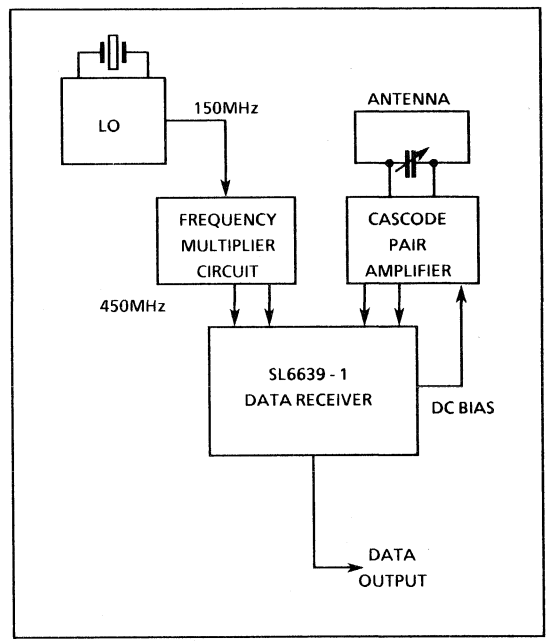


Fig.1 Block Diagram

THE EXTERNAL AMPLIFIER (Fig. 3.)

Unlike the internal amplifier the low cost external cascode amplifier Fig.3 is not feed from the internal current source - R1 is used to set an extra 1mA in the amplifier.

The external amplifier is basically a copy of the internal amplifier, however a little more current has been used with transistors of type BFR92A to cope with the extra speed requirement. (surface mount components where used). The two base voltages required for the external cascode amplifier are available on external pins of the SL6639-1 ie Pin 5 = 1.2V and Pin 4 = 1.0V. This reduces the additional components used down to the transistors and two resistors.

If transistors of sufficient gain at 500μA can be afforded then the external amplifier can be configured as an exact copy of the internal amplifier, dynamic range and low current consumption can then be maintained.

DYNAMIC RANGE

For some applications dynamic range is of great concern. This is especially the case for systems using high transmitter power with either mobile transmitters or receivers.

This problem has been overcome in the low cost solution (Fig.3) using a low cost PNP transistor.

As described earlier the current source accessible on pin 20 of the SL6639 - 1 will be switched off by the onchip SL6639-1 AM detector well before the mixers reach overload. Within the external amplifier (Fig. 3.) the 500μA current source is used to hold the PNP (T3) on. This transistor then connects the amplifier to the supply. When the current source on pin 20 is switched off, the PNP transistor disconnects the amplifier from the supply, however the radio will still function on crosstalk through the amplifier. [Note this will save on power if the receiver is close to the transmitter.]

If the input signal never exceeds -40dBm the PNP transistor T3 and R2 can be removed. The circuit is then connected directly to the supply in the normal way. An extra 500μA supply current will then be saved.

THE TRANSFORMER

The two mixers within the SL6639-1 require 180° phase shifted inputs. The simplest way to achieve this is with a transformer. In fact this task is simplified at high frequency as only one single turn about 4mm diameter is used for the primary and two turns of the same diameter used for the secondary. [Note it should be possible to etch this transformer onto the PCB].

The primary of this transformer is tuned using a 0.9 to 2pF capacitor. This tuning is performed by monitoring Pin 28 of the SL6639-1 (low frequency). With a low level input signal., Pin 28, pk-pk voltage is adjusted for maximum.

The secondary winding of the transformer is not critical, one or two turns should suffice.

LOCAL OSCILLATOR

As we are now using the device at frequencies above that of generally available crystals .The standard technique using one of the higher harmonics of the local oscillator is now required. (Frequency multiplier).

A tuned collector load transistor following a Colpits oscillator which uses a 150 MHz crystal will satisfy this requirement. Fig. 4 shows a prototype oscillator working at low supply voltage.

RECOMMENDED SPECIFICATION

FSK Data
Data Rate 500BPS
Modulation ± 4.5kHz
Carrier frequency 418.0MHz
Supply 3V
Load on Data Output 50KΩ
Antenna Loop at right angles to local oscillator
Local oscillator level -25dBm
Phase Shift Capacitors 3.9pF with 100 OHm

Devised by Plessey Field Applications Department Swindon.

FREQUENCY 'V' SENSITIVITY

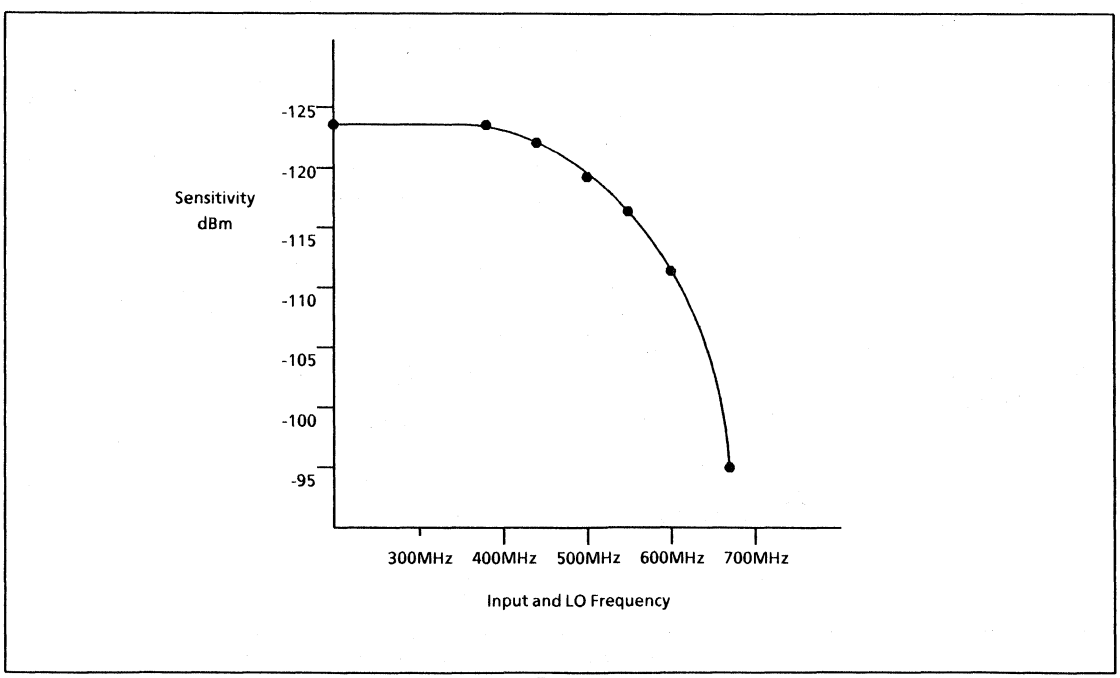


Fig. 2.

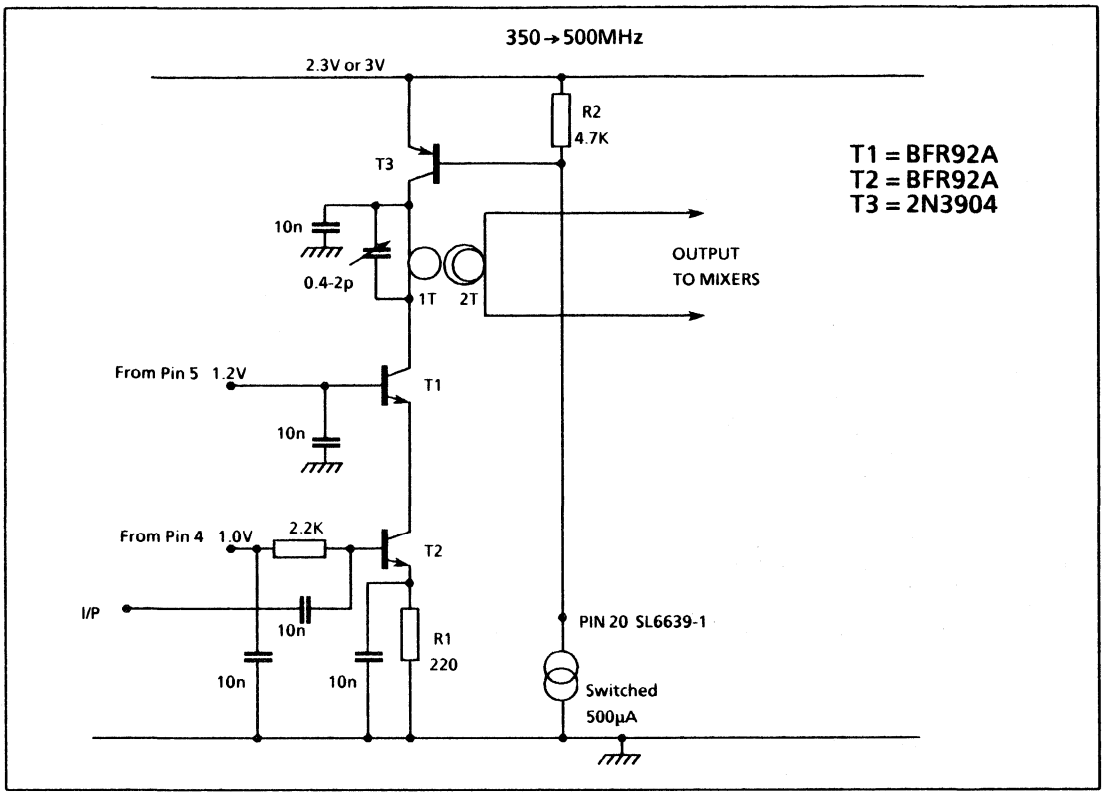


Fig. 3. SL6639-1 External Amplifier With AGC

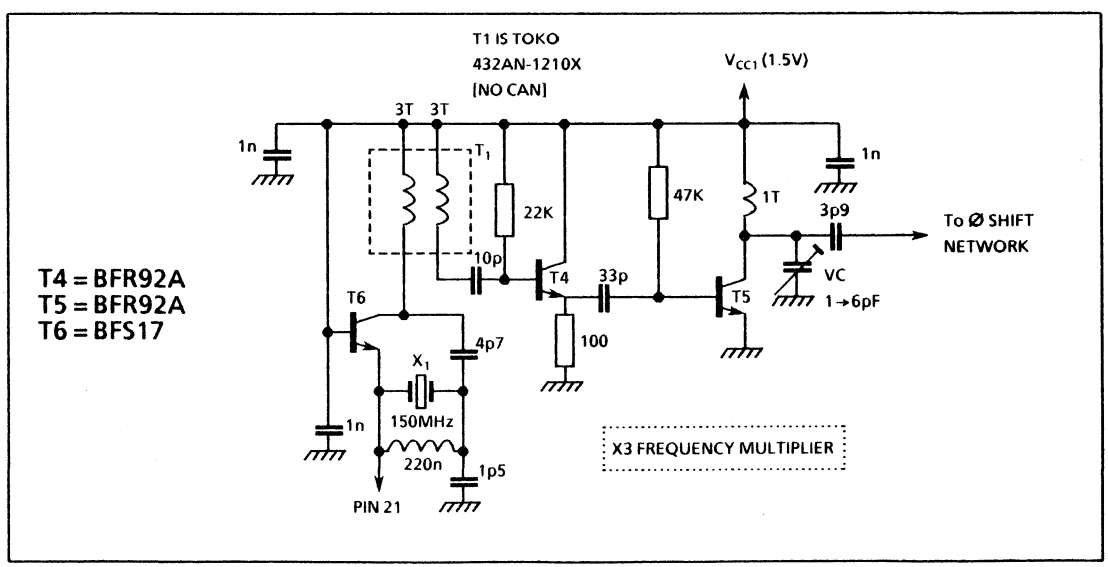


Fig. 4. Prototype 450MHz Local Oscillator For Low Voltage Operation

SL6442

APPLICATION CIRCUIT FOR USE AT 950MHz

This Application Note describes a circuit configuration which demonstrates the functions and performance of the SL6442 which is a 1GHz amplifier/mixer receiver front end

A functional block diagram is shown in Fig. 1 and illustrates the main circuit elements.

Fig. 2 is a schematic diagram which illustrates the arrangement of the ancillary components required for optimum performance at 950MHz. Approximate starting values for these components were obtained using a Smith chart and data derived from s-parameter analysis of the SL6442.

The SL6442 contains a low noise amplifier which may be gain controlled by a D.C. signal, and two identical mixers suitable for either direct conversion I & Q receivers or image cancelling superhet receivers. There is also a battery economy facility. The device operates from a nominal 5V supply and draws about 4mA when powered up.

The actual component values were determined by using a linear circuit simulator such as Touchstone™. In this case the circuit is optimised for maximum gain and minimum input reflection coefficient at the required frequency.

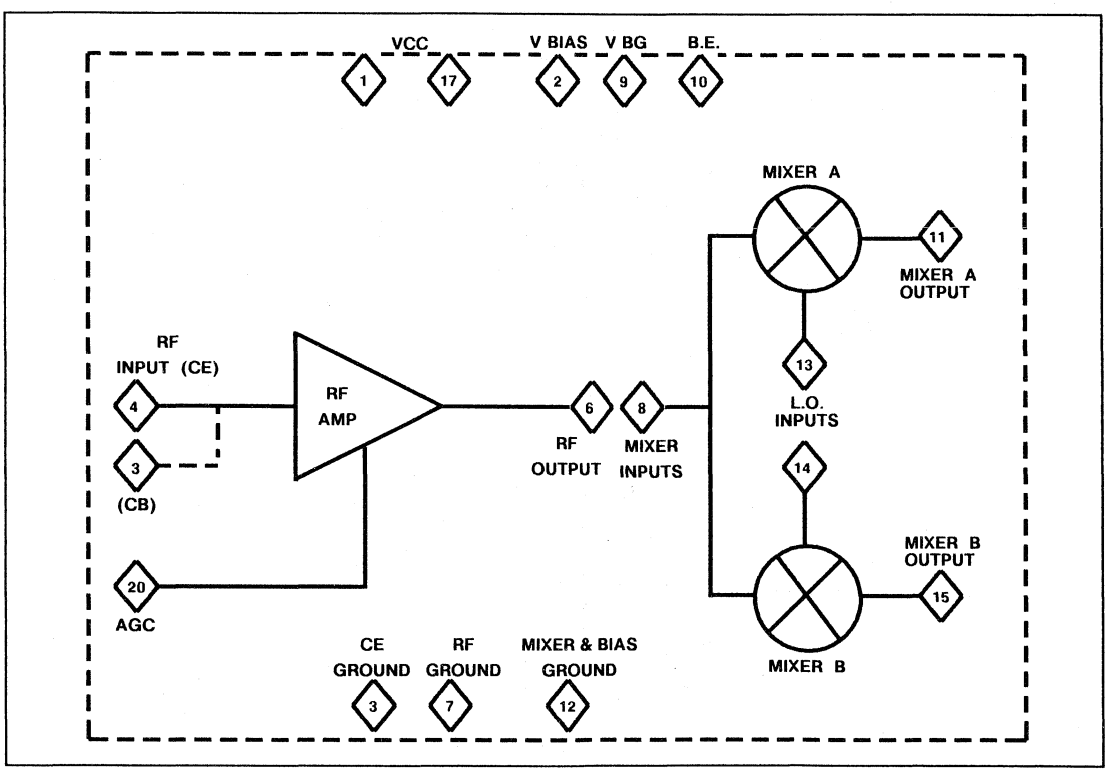


Fig.1

The input match is achieved by using a stripline shorted stub network. The LNA output to mixer input match is accomplished by using a series inductor and the mixer output to 50ohm match consists of a tunable LC network.

To prevent possible RF instability, pin2 (V bias) is decoupled with a series RC network as well as a 2.2μF capacitor. The quadrature phase shift network consists of phase lead and phase lag RC 'L' networks, which are capacitor coupled to the L.O. input pins. Inductor L3 serves to resonate out the parasitic capacitance between the two ports.

The exact values of the phase shift components have been determined empirically and the ones shown in the circuit diagram achieve an amplitude and phase imbalance of about 1dB and 4 degrees respectively.

The variable capacitors VC1 and VC2 are tuned for a maximum output level at an I.F. of 20MHz. Other I.F frequencies may require changing the values of the trimmers and/or L4 and L5. At zero I.F as in direct conversion receivers the output matching network is transparent.

If the AGC facility is not required it is necessary to connect pin 20 to pin 9 (VBG). The battery economy pin may be connected directly to ground if power down is not used.

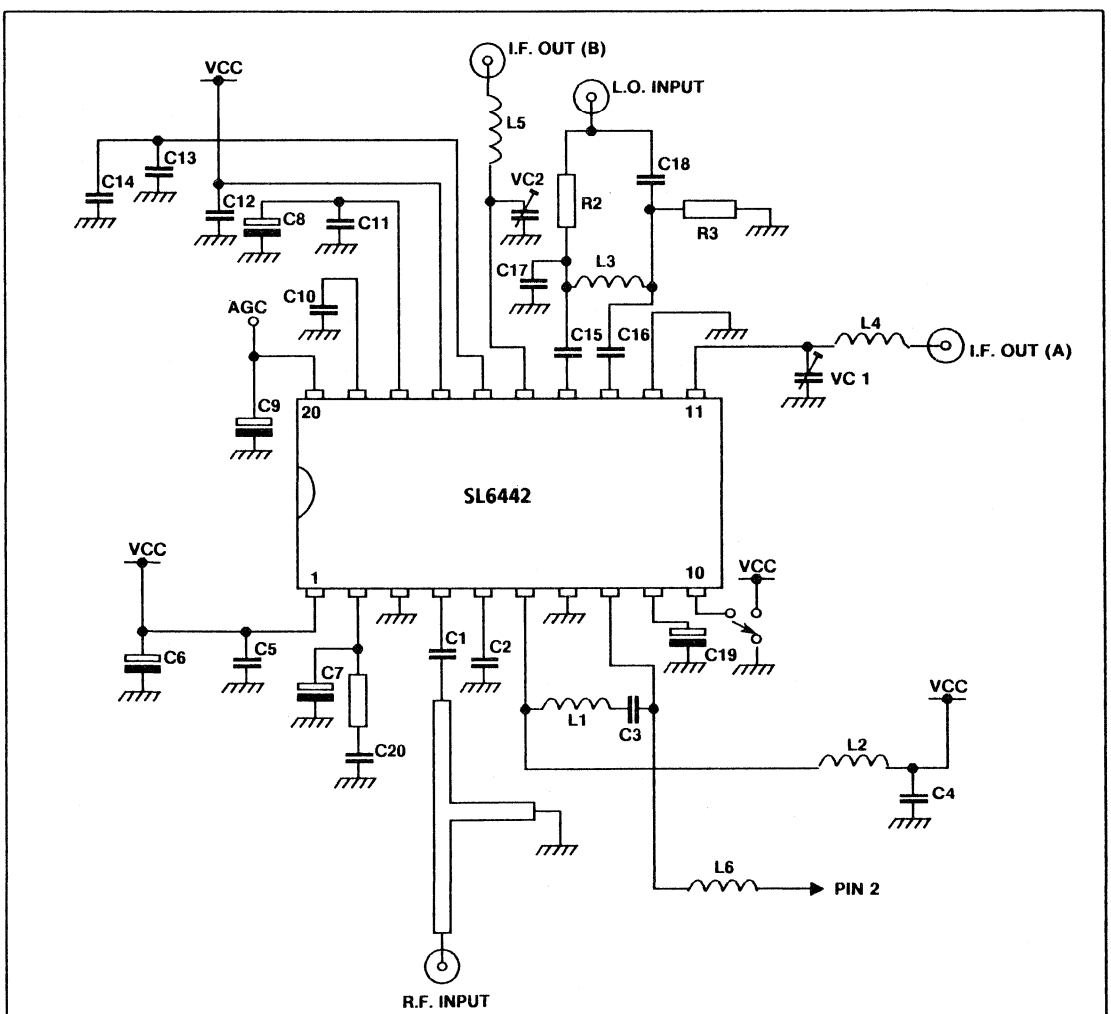


Fig. 2 Circuit diagram

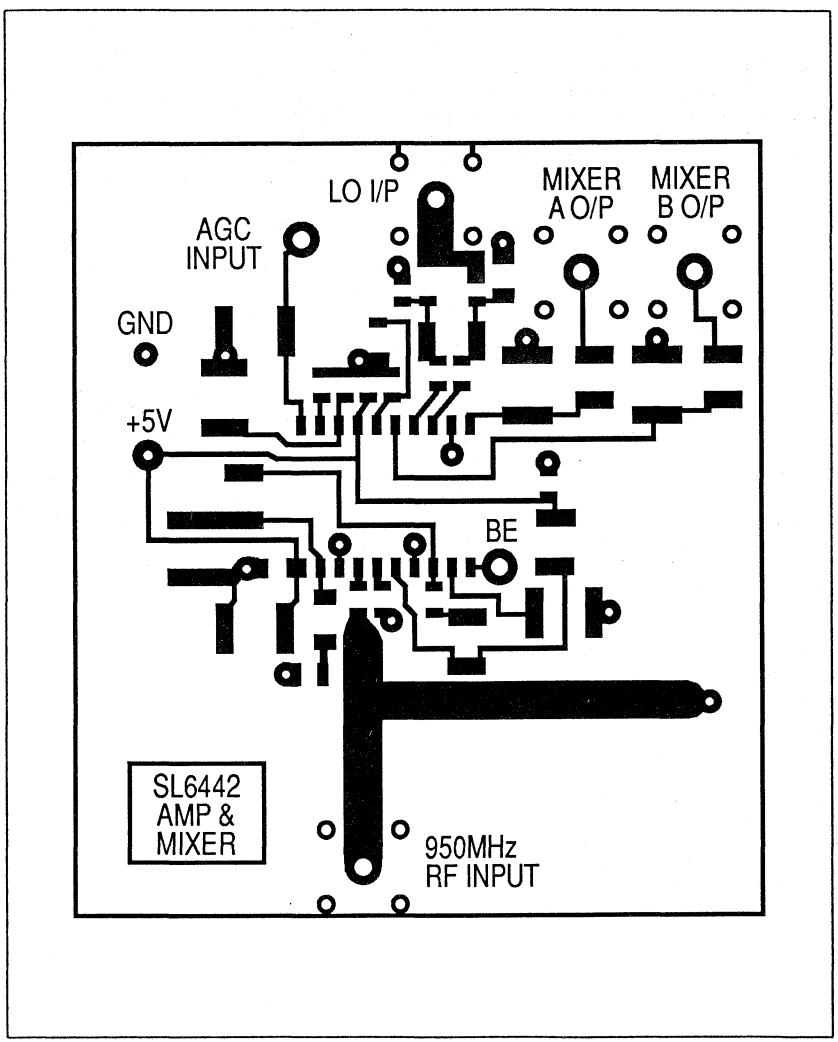
PERFORMANCE CHARACTERISTICS

MEASUREMENT CONDITIONS:

VCC = 5·0V. Vagc = 1·20V.
Input/Output terminations = 50ohm
L.O. drive level (into phase shift network) = -5dBm
Temperature = 25°C

RESULTS	
Overall power gain (20MHz I.F.)	7dB
Overall voltage gain (baseband)	33dB (ZL > 100k)
3rd. order input intercept (20MHz I.F.)	-22dBm
Overall DSB noise figure (20MHz I.F.)	8·2dB

The actual pcb layout and component values are shown in Fig. 3.



RI, R3	47Ω
R2	51Ω
C1	27p
C2, C5, C10	
C11, C13, C15	18p
C16, C20	
C3, C4	22p
C6, C7, C8	
C9, C19	2µ2
C12	In
C14	100n
C17	3p3
C18	5p6
L1	10n
L2	100n
L3	15n
L4, L5	3µ3
L6	82n
VC1, VC2	2-20pF

Fig. 3

USING THE SL6649-1 IN LOW PROFILE APPLICATIONS AT FREQUENCIES BELOW 200MHz

INTRODUCTION

This Application Note describes the use of the SL6649-1 at frequencies below 200MHz. A new circuit design has been used which eliminates the transformers that were used in previous demonstration boards for this device. This has the benifit of being able to use small, low profile components enabling a receiver to be built with a maximum component height of 2mm. (using the low profile chip carrier package).

The AC characteristics given in the SL6649-1 data sheet are based on the use of transformer matching from the RF amplifer to the mixer. Use of the transformerless circuit can result in a lower front end gain and thus may degrade the overall receiver performance. Improved perfromance may be achieved by the use of an external low noise, high gain transistor amplifier in place of the on-chip cascode arrangement.

RF AMPLIFIER

The on-chip amplifier consists of two transistors configured in cascode. This is illustrated in Fig.1. Bias is provided by a current source on pin 20 and the voltage V_{BG} and V_R via R1. At high signal levels this current source is dependent on the R.F. level at the mixer inputs and can therefore provide an automatic gain control (AGC) function.

Pin 20 is decoupled to ground by a 1nF capacitor. The upper transistor being in common base has its base decoupled to ground by a 1nF capacitor.

The input to the cascode is matched to a 50 Ohm source by a single series inductor (L3). It is also wise to include a 1nF dc blocking capacitor (C11) between the signal source and the input circuit. The output load is a tuned circuit with a capacitor tap to match the combination of an LC phase shift network (L5 and C21) and the differential mixer inputs. The component values for the LC phase shift network are chosen to give equal amplitude and 180 degrees phase shift between the mixer R.F. inputs. This circuit will be dependant on the impedance of the mixer input. Some experimentation with the values of L5 and C21 may be necessary to achieve optimum gain and intermodulation performance.

The internal cascode amplifier works optimally at frequencies up to 200MHz. Above 200MHz the receiver will work with reduced sensitivity due to the bandwidth and noise figure limitations of the internal amplifier. For use at frequencies up to 500MHz where high performance is required, an external amplifier is recommended.

LOCAL OSCILLATOR

The L.O. which is shown in Fig. 2, uses an external transistor which is connected to a 280µA current source on pin 21 of the SL6649-1 via inductor L6. The oscillator feedback circuit comprises a capacitor tap (VC2, C23 and C18) and a series resonant crystal which is shunted by an inductor (L4) to suppress oscillation at the crystal fundamental frequency by tuning out the holder capacitance. The base of the transistor is connected to $V_{CC}1$ and decoupled to ground by a 1nF capacitor. The collector circuit is designed to be resonant at the required oscillator frequency and the output signal is fed to an RC quadrature network consisting of R6, R7, C13 and C15 via a capacitor (C17) and then to the mixer L.O. input ports. This RC network is designed such that R and the reactance of the capacitor, C, equals 100 Ohm at the wanted frequency.

OVERALL RECEIVER CIRCUIT

The complete receiver block schematic is shown in Fig. 3 and illustrates the remaining ancillary components which are not dependant on the RF frequency used.

RECEIVER ALIGNMENT

Monitor the output at pin 28 of the device with an oscilloscope set to 20mV/div. (A.C. coupled). Feed the R.F. input from a 50 Ohm signal generator set at the nominal crystal frequency at a level of about 20µV (-80dBm). Tune VC2 for a zero beat at pin 28 (channel B test). Now offset the generator frequency by 2-3 KHz, this should give a sine wave output of about 50mV p-p. Tune VC1 for a maximum at the pin 28 test point.

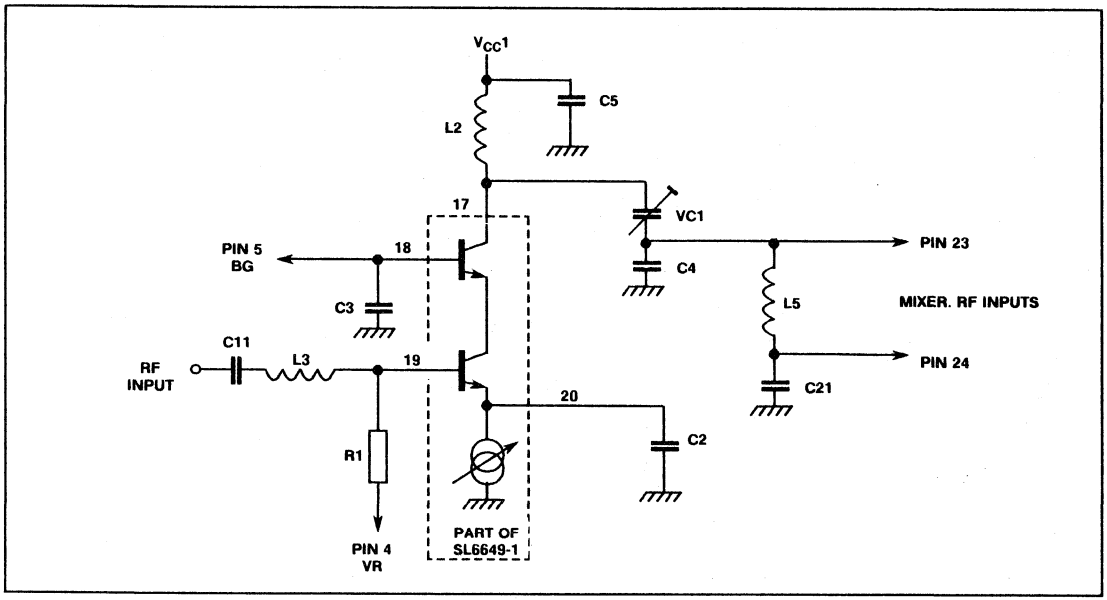


Fig. 1 R.F. amplifier

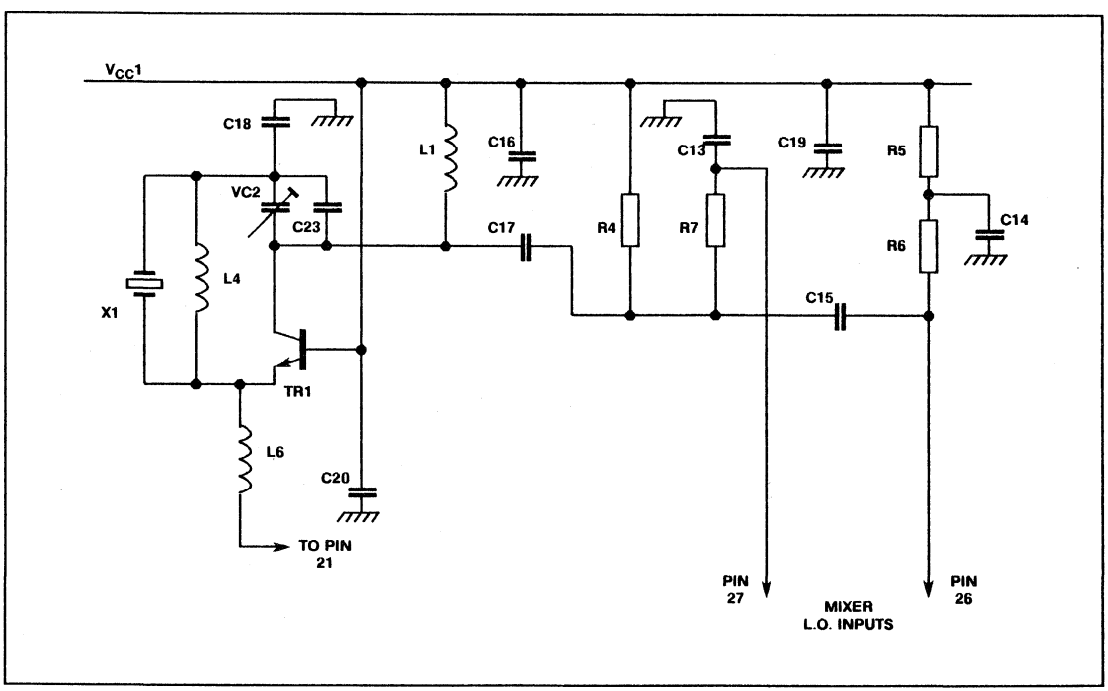


Fig. 2 Local oscillator

COMPONENTS	50MHz	153MHz	173MHz
C1	1nF	1nF	1nF
C2	1nF	1nF	1nF
C3	1nF	1nF	1nF
C4	-	22pF	33pF
C5	22nF	1nF	1nF
C6	2.2µF	2.2µF	2.2µF
C7	2.2µF	2.2µF	2.2µF
C8	1nF	1nF	1nF
C9	2.2µF	2.2µF	2.2µF
C10	2.2µF	2.2µF	2.2µF
C11	1nF	1nF	1nF
C12	1nF	1nF	1nF
C13	33pF	10pF	10pF
C14	1nF	1nF	1nF
C15	33pF	10pF	10pF
C16	1nF	1nF	1nF
C17	3.3pF	3.9pF	3.9pF
C18	18pF	4.7pF	1.5pF
C19	1nF	1nF	1nF
C20	1nF	1nF	1nF
C21	33pF	10pF	10pF
C23	39pF	-	-

COMPONENTS	50MHz	153MHz	173MHz
L1	470nH	100nH	100nH
L2	1µH	100nH	100nH
L3	390nH	100nH	100nH
L4,	-	220nH	220nH
L5	470nH	150nH	100nH
L6	10µH	10µH	10µH
R1	2.2K	2.2K	2.2K
R2	270K	270K	270K
R4-R7	100	100	100
R8	100K	100K	100K
TR1	BFS17	BFS17	BFS17
TR2	BFS17	BFS17	BFS17
VC1	1.5-10pF	1.5-10pF	1.5-10pF
VC2	1.5-10pF	1.5-10pF	1.5-5pF
X1	50MHz series res.	153MHz series res.	173MHz series res..

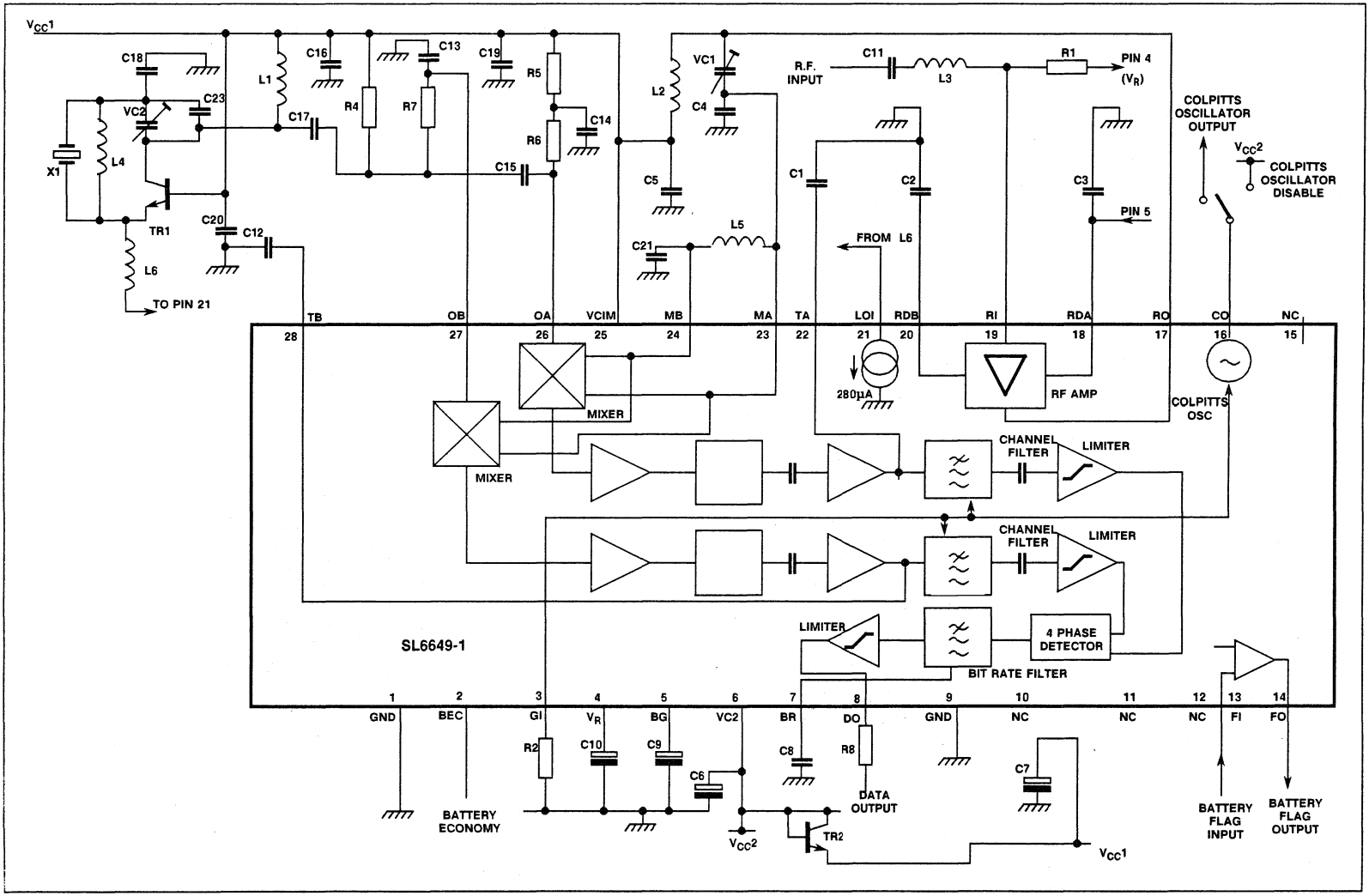
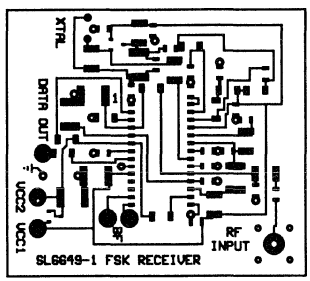
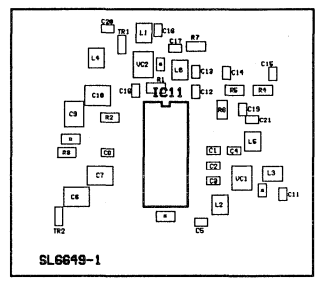


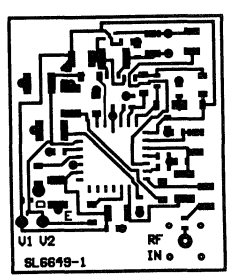
Fig. 3. Circuit diagram of receiver

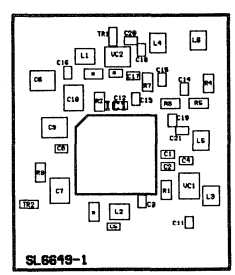
P.C.B. LAYOUTS
MP PACKAGE





P.C.B. LAYOUTS
LC PACKAGE





SL2365 Applications

The SL2365 is an array of transistors configured to form a dual long-tailed pair with tail transistors which are current mirrored to similar transistors whose bases and collectors are connected internally.

The ICs are manufactured on a very high speed bipolar process which has a typical f_t of 5 GHz. The device is available in a surface mounted miniature plastic DIL package (MP14), the pin connections of which are shown below.

Various applications are described including a 900 MHz amplifier, a frequency doubler, a frequency tripler and a single balanced mixer.

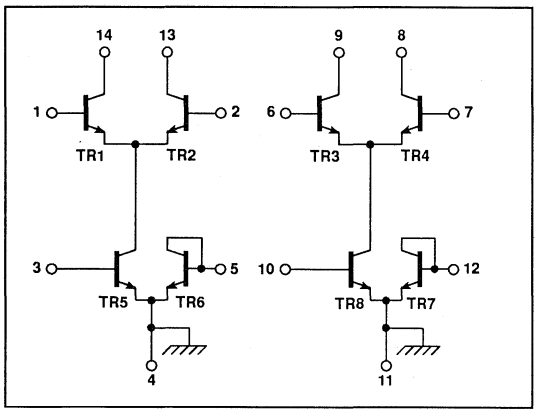


Fig. 1 SL2365 schematic diagram

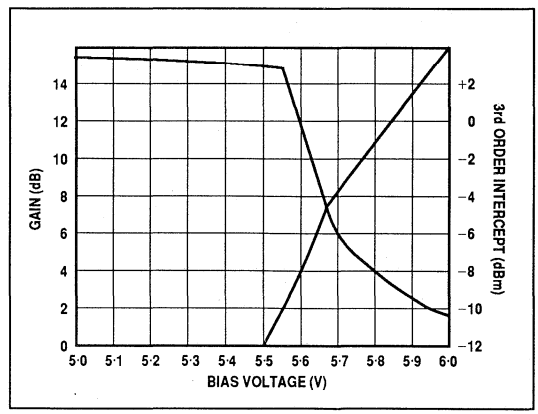


Fig. 3 Third order intercept at gain of 12.5dB (using current mirror at 4mA) = −7dBm

A 900MHZ GAIN CONTROLLED AMPLIFIER

In Fig. 2 the collecter load of TR1 is a transformer composed of a 14mm length of 75Ω stripline resonated with a 1-6pF variable capacitor. The secondary of the transformer is a small loop of stiff wire grounded at one end and located a few millimetres above the stripline. The gain and 3rd order intercept versus V_{bias} is shown in Fig.3. The noise figure at full gain is 9dB.

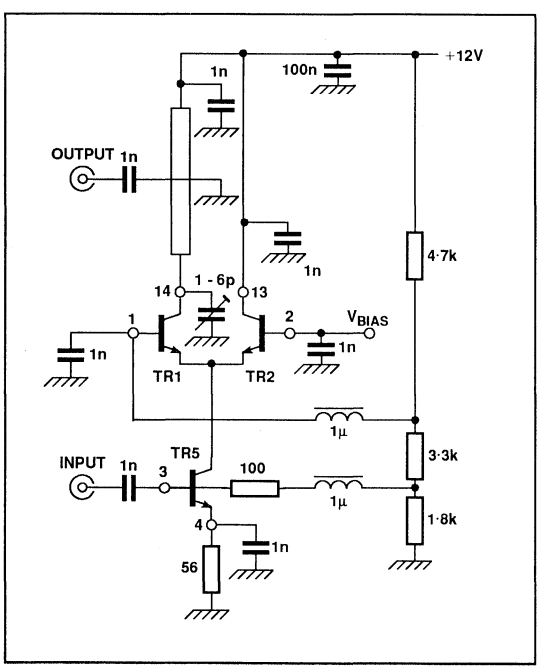
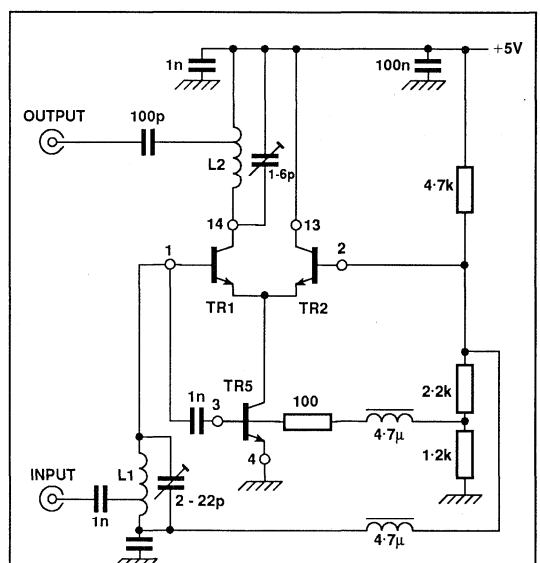


Fig. 2

A 150-300MHz FREQUENCY DOUBLER

The frequency doubler, Fig. 4, has a gain of +1dB for a −20dB input and input frequency rejection of 18dB.



NOTES

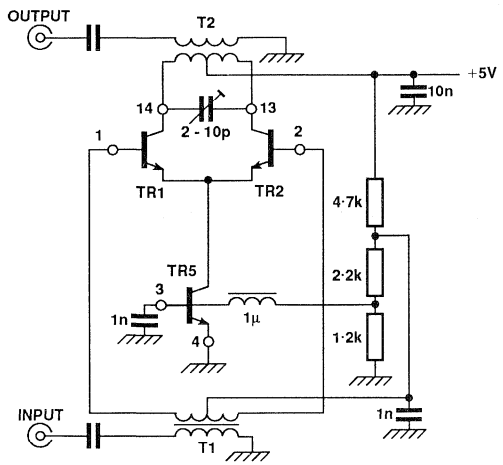
L1 = 4turns 20 swg tinned wire, 5mm diameter, tapped 1 turn from ground end.

L2 = 3 turns 20 swg tinned wire, 5mm diameter, tapped 1 turn from 5V rail end.

Fig. 4

A 100--300MHz FREQUENCY TRIPLER

Fig. 5 shows a 100-300MHz frequency tripler with a gain of −40dB, input frequency rejection of 30dB, and second harmonic rejection of 28dB.

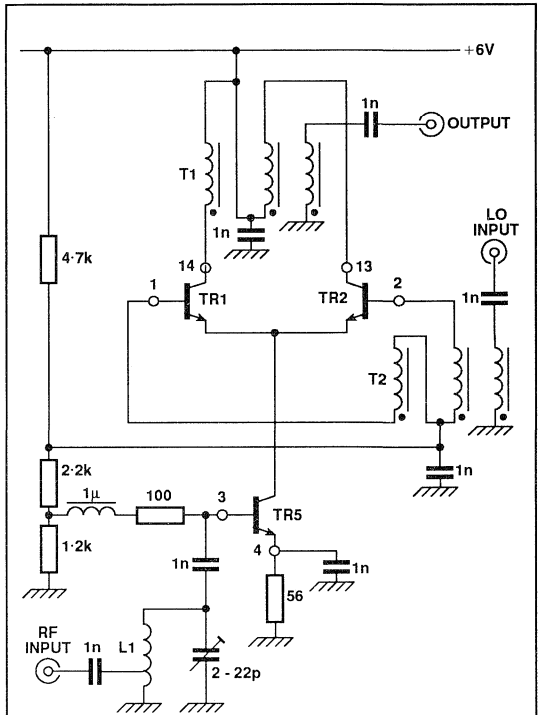


NOTES
T1 primary = 4 turns 36 swg enamelled wire, wound on ferrite core.
T1 secondary = 4 turns 36 swg enamelled wire, wound on LF ferrite core (twisted pair).
T2 primary = 2 turns 20 swg tinned wire, 5mm diameter.
T2 secondary = 4 turns 20 swg tinned wire, 5mm diameter, positioned axially relative to T2 primary.

Fig. 5

A SINGLE BALANCED MIXER

The mixer of Fig. 6 has a gain of 13dB, 3rd order intercept of −13dBm (−10dBm using 2mA in current mirror) and noise figure of 10dB.



NOTES
L1=4turns 20 swg tinned wire, 5mm diameter, tapped 1 turn from ground end.
T1 and T2 = 4 turns of trifilar wound 36 swg enamelled wire, wound on LF ferrite core.

Fig. 6

Multimodulus Division

This Application Note compares the various techniques currently employed in phase locked loop (PLL) frequency synthesiser designs with the technique of multimodulus division embodied in the GPS NJ882X series of synthesiser controllers when combined with the SP87XX series of two-modulus prescalers.

DIRECT DIVISION

Phase Locked Loop Frequency Synthesisers of the form shown in Fig. 1 suffer from the problems inherent in producing fully programmable dividers required to operate at appreciable frequencies while not consuming excessive power. Although advances in small geometry integrated circuit technology make any figures obsolescent, guaranteed operation above about 50MHz still requires relatively high power.

FIXED PRESCALING

Fixed prescaling, as in Fig. 2, is widely used, but for a division ratio of P in the prescaler, the phase comparison frequency of Fig. 1 has been reduced by a factor of $1/P$. This lower frequency necessitates a lower bandwidth in the phase locked loop, and thus a greater susceptibility to microphonics etc., and, generally speaking, a longer lock-up time.

MIXING IN THE LOOP

One alternative to fixed division is mixing, as in Fig. 3. The use of mixers requires great care in the choice of frequencies if spurious products are not to be a problem and although widely used, it is certainly complicated in terms of its physical realisation, requirements for 'adjust on test' parts, and in its susceptibility to layout problems.

MULTIMODULUS DIVISION

The multimodulus divider system, shown in Fig. 4, is significantly less complicated. It is built up from a number of blocks.

1. A two-modulus prescaler which will divide by one of two numbers P or $P + 1$ (e.g., 10/11, 64/65 etc.).
2. A programmable 'A' counter, the output of which controls the modulus of the prescaler.
3. A programmable 'M' counter which is clocked in parallel with the 'A' counter. In most of the NJ882X series, the output of the 'M' counter resets both itself and the 'A' counter (see Fig. 4).
4. A programmable Reference Frequency counter, 'R', the division ratio of which is determined by the reference frequency f_{osc} and the desired channel spacing (see below).

Principle of Operation

The 'A' counter is programmed to a smaller number than the 'M' counter, and assuming the counters to be empty, the system starts with the prescaler ($P/P + 1$) dividing by $P + 1$. This continues until he 'M' counter is full. As the 'M' counter has received A pulses, this counter overflows after $(M - A)$ pulses, corresponding to $P(M - A)$ input pulses to the divider. Thus the total division ratio N is given by:

$$N = (P + 1)A + P(M - A) = PM + A$$

Obviously, A must be equal to or less than M for the system to work, while for every possible channel to be available, the minimum total divide ratio is $P(P - 1)$ while the maximum total division ratio is $M(P + 1)$. A_{max} should be $\geqslant P$.

Although simple in theory, there are a few points which require consideration in the design of such a divider system. Of these probably the most important is Loop Delay.

Consider the counter chain at the instant that the $(P + 1)$th pulse appears at the two-modulus prescaler input. After some time $tp1$ the output produces a pulse, which clocks the A and 'M' counters. Assume that the 'A' counter is filled by the pulse, and so after a time t_{p2} (determined by the propagation delay of the 'A' counter), an output is produced to set the two-modulus prescaler ratio to P. After a set time t_s, the dual modulus divider will divide by P. But if $t_{p1} + t_{p2} + t_s$ is greater than P cycles of input frequency, the divider will not be set to divide by P until after P pulses have appeared, and the system will fail.

$$\text{Thus, } \frac{P}{f_{VCO}} > \text{total loop delay}$$

Design in this region is critical: worst case tolerances MUST be used if the reproducibility of the design under temperature and voltage extremes is not to be compromised.

The value of P must also be large enough that the output frequency from the prescaler does not exceed the maximum input frequency of the following circuitry. In single-chip MOS controllers this may well be as high as 50MHz under some conditions, but under others, such as high temperature and low voltage, much lower. Generally, however, the limitation on such circuits is the loop delay rather than input frequency.

The loop delay is affected by the edge of the waveform on which the divider and the 'A' and 'M' counters trigger. If the edges are opposite then the loop delay may be increased by a large amount, and if in these circumstances, the use of an inverter at the output of the divider is justified.

The minimum value of P is therefore settled by these constraints, but the actual choice of P may be determined by the ease of programming. This may be seen by considering a synthesiser with a 25kHz phase comparison frequency (channel spacing) f_{comp}, using a ÷40/41 prescaler.

At 156MHz:

$$N = 156/0{\cdot}025 = 6240$$

therefore $PM + A = 6240$

$40M + 0 = 6240$ ($A = 0$ for the lowest channel)

$M = 156$

In general, where

f_{VCO} $P = 1$ or 10 or 100

$M = f_{VCO}$, $f_{VCO} \div 10$, $f_{VCO} \div 100$ etc.

and similarly for the binary division ratios.

The choice of prescaler is therefore determined by:

1. VCO frequency
2. Total loop delay.
3. Prescaler output frequency must be within the controller input frequency band.
4. Programming ease.

REFERENCE FREQUENCY DIVISION RATIO (R)

The value of R is set by the input frequency and the phase comparison frequency. Higher input frequencies require greater power and offer lower stability, while lower frequencies (below 4MHz) generally require larger physical crystal sizes. Normally a frequency between 4 and 15 MHz is used, especially as in double conversion equipments commonality of oscillators may be possible. For example, with a 5kHz comparison frequency and 10·240MHz 2nd local oscillator frequency,

$$R = \frac{(10{\cdot}240 \times 10^6)}{(5 \times 10^3)} = 2048$$

Note that, for the NJ882X series, the reference counter division ratio is twice the programmed value and is therefore always even (see AN133 and individual data).

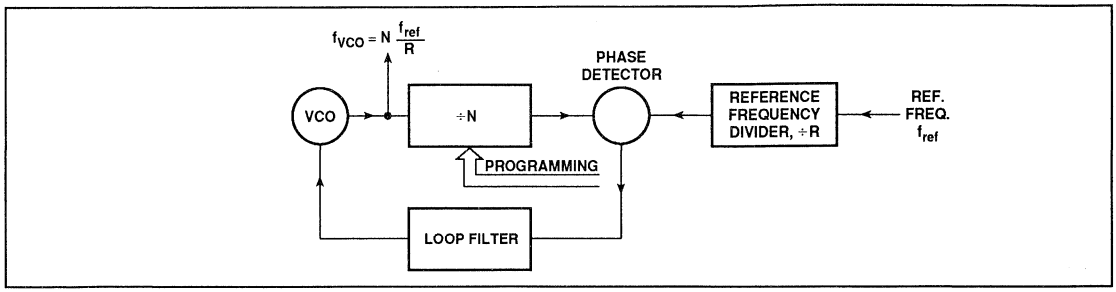


Fig. 1 Direct division

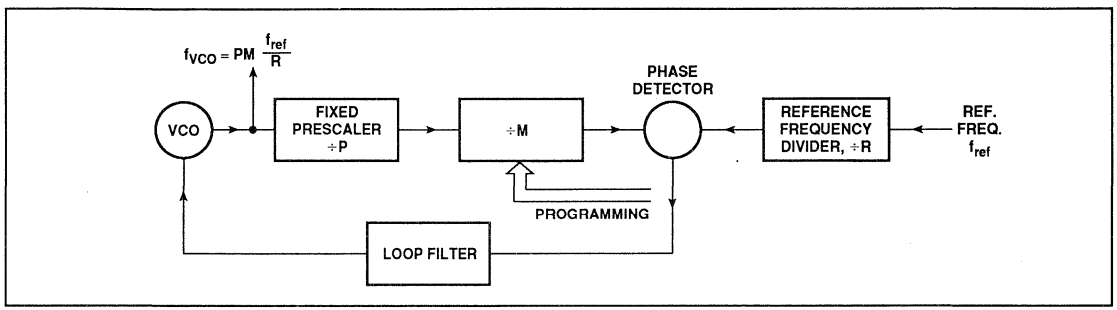


Fig. 2 Fixed prescaling

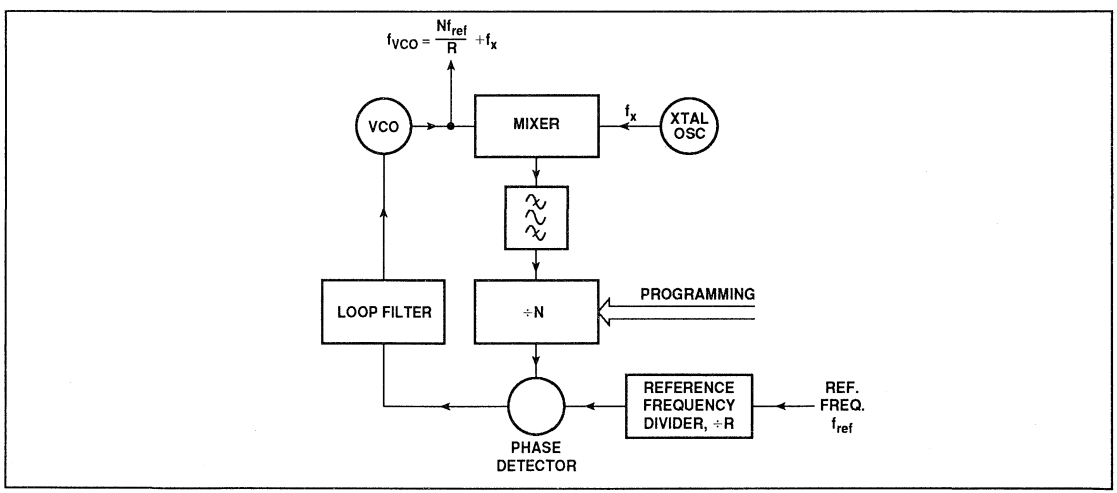


Fig. 3 Mixing in the loop

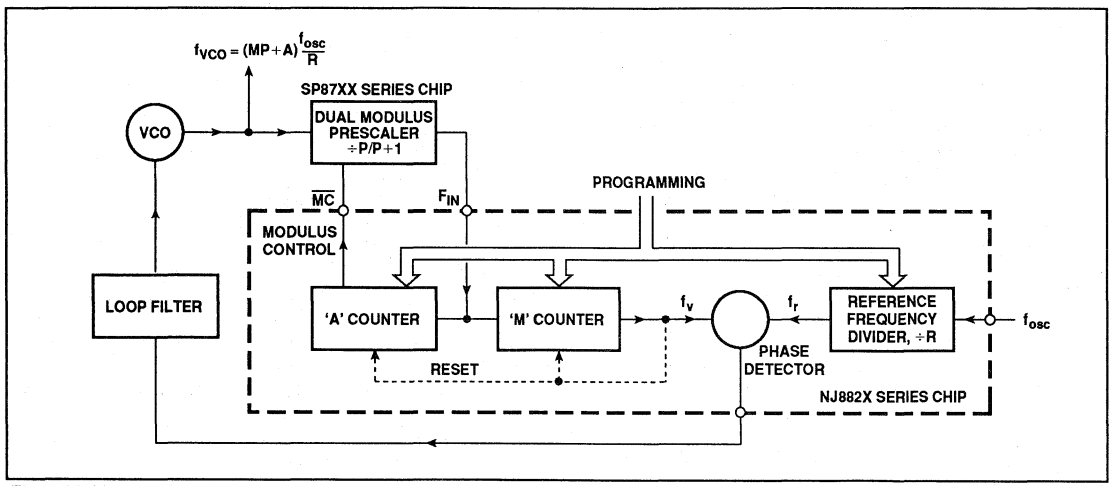


Fig. 4 Multi- modulus division. The NJ8823, NJ88C24 and NJ88C28 have non-resettable counters for faster loop lock-up times; see individual data.

Programming the NJ8820 and NJ8821/23

The NJ8820, NJ8821 and NJ8823 are versatile high performance CMOS frequency synthesiser controllers. The differences between devices are in hardware programming methods.

The basic system of a single loop frequency synthesiser is shown in Fig. 1, where a 2-modulus prescaler is used to divide the VCO frequency down to a suitable range for use in the CMOS device. The NJ8820/1/3 is programmed by 8 4-bit words on the data inputs: the addresses for these words may be obtained internally or externally and appear on the Data Select inputs/outputs. To program any frequency, it is necessary to program the 'A' counter (7 bits), the 'M' counter (10 bits) and the reference or 'R' counter (11 bits).

ADDRESSING

Addressing is by one of three modes. These are:

A. Self Programming Internal Mode

Here the reference oscillator (either an internal crystal oscillator or from an external source) signal is divided in the reference counter by 64 and a Data Read cycle commences every $1024/f_{osc}$ seconds.

In this Data Read cycle the Memory Enable pin ($\overline{ME}$, NJ8820 only) is pulled low, and the Data Select outputs DS0, 1 and 2 count in binary from 0 to 7. This provides addresses for the data on D0, 1, 2 and 3, the data being transferred to internal latches on the trailing edges of the Data Select pulses (see Fig. 2). Note that the Program Clock is internally derived and is at a frequency of fosc/64. The PE (Program Enable) pin is grounded, and the cycle continuously repeats. This mode is not recommended, however, as noise from the digital data may be picked up by the phase locked loop.

B. Single Shot Internal Mode

In this mode, the PE pin is provided with a pulse input which initiates a data read cycle as outlined above; on the NJ8820, the $\overline{ME}$ pin goes high at the end of the cycle, thus minimising power consumption . 'Power-on' initiation is used, in which the application of power to the device is sensed and a programming cycle initiated. In order to avoid corruption of the data, a delay of 53248 cycles of reference oscillator frequency is provided before the programming cycle occurs. This delay is approximately 5ms for a 10MHz reference frequency.

C. External Mode

The address is presented to DS0, 1 and 2, and a pulse is applied to the PE pin to transfer data to the internal latches. The data is transferred from the latches to the counters simultaneously with the transfer of data into Latch 1: thus this word should be the last one to be entered.

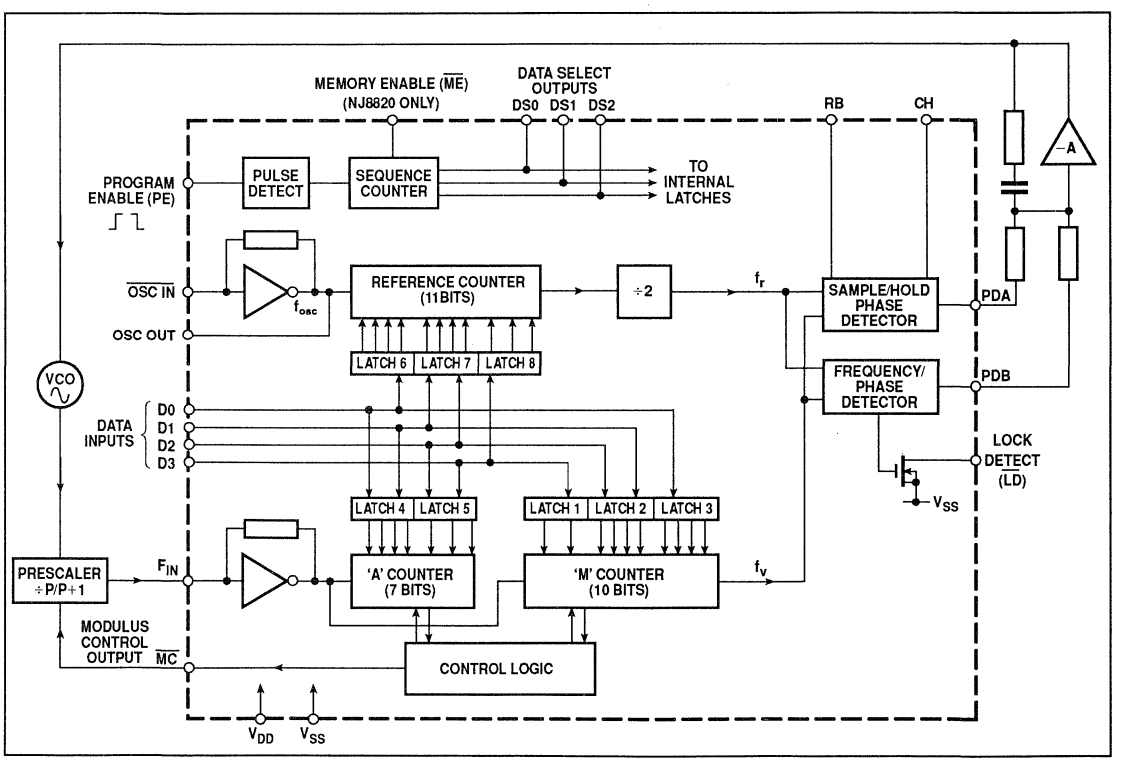


Fig. 1 The phase locked loop

WORD VALUES

For any particular set of conditions — namely operating frequency, prescaler ratio, comparison frequency and input frequency from the reference oscillator — a unique set of programming words exists.

Reference Divider

This divider produces the comparison frequency required by the synthesiser. The division ratio is programmable from 6 to 4094 in steps of 2, the programmed number being half the division ratio. Therefore, if for example a 10MHz crystal is used, and a 12·5kHz comparison frequency is required, this counter would be programmed to give a ratio of 100000 ÷ 12·5 = 800. The actual programmed number would thus be 400, entered in binary according to the data map, Table 1.

Word	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Table 1 Data map

'A' and 'M' Counters

The 'A' counter is a 7-bit counter and the 'M' counter is a 10-bit counter. The programming calculations are as follows:

1. The 'A' counter should contain x bits such that $2^x = M$.

2. If more bits are included in the 'A' counter, these should be programmed to zero.

e.g. $M = 64 = 6$ bits
$A = 10$ bits
then the 4 MSB are programmed to zero.

3. The 'M' and 'A' counters are treated as being combined so that the MSB of the 'M' counter is the MSB of the total and the LSB of the 'A' counter is the LSB of the total.

For example, a synthesiser operating from 430 to 440MHz in 25kHz steps uses a 64/65 divider, and the control circuit uses binary counters.

$N = f/f_r$ where f_r = channel spacing = 25kHz
$N_{min} = 430/0{\cdot}025 = 17200$
$N_{max} = 440/0{\cdot}025 = 17600$

Minimum possible division ratio is $P^2 - P = 4032$ where P is the two modulus prescaler ratio.
Maximum allowable loop delay = $64/(440 \times 10^6) = 145$ns.

Total division ratio, N, is given by
$N = PM + A$
$P = 64$, as a 64/65 prescaler is used
N_{min} from above is 17200
Therefore $17200 = 64M + A$
and $M \geqslant A$.
Let $A = 0$ then $M_{min} = 17200 \div 64 = 268{\cdot}75 = 268$
and $M_{max} = 17600 \div 64 = 275{\cdot}0$

Thus the' M' counter must be programmable from 268 to 275 as required: the 'M' counter must have at least 9 bits.
For a frequency of 433·975MHz
$N = 433{\cdot}97 \div 0{\cdot}025 = 17359$
therefore $M = 17359 \div 64 = 271{\cdot}2343$
The 'A' counter is programmed for the remainder i.e.
$0{\cdot}2343 \times 64 = 15$
From this, the 'A' counter is programmed to 15 and the 'M' counter to 271. The output frequency can now be checked.
$N = PM + A$
$= 271 \times 64 + 15 = 17359$
and this is the required frequency divider ratio.
Repeated calculations for memory programming may be easily evaluated using a programmable calculator.

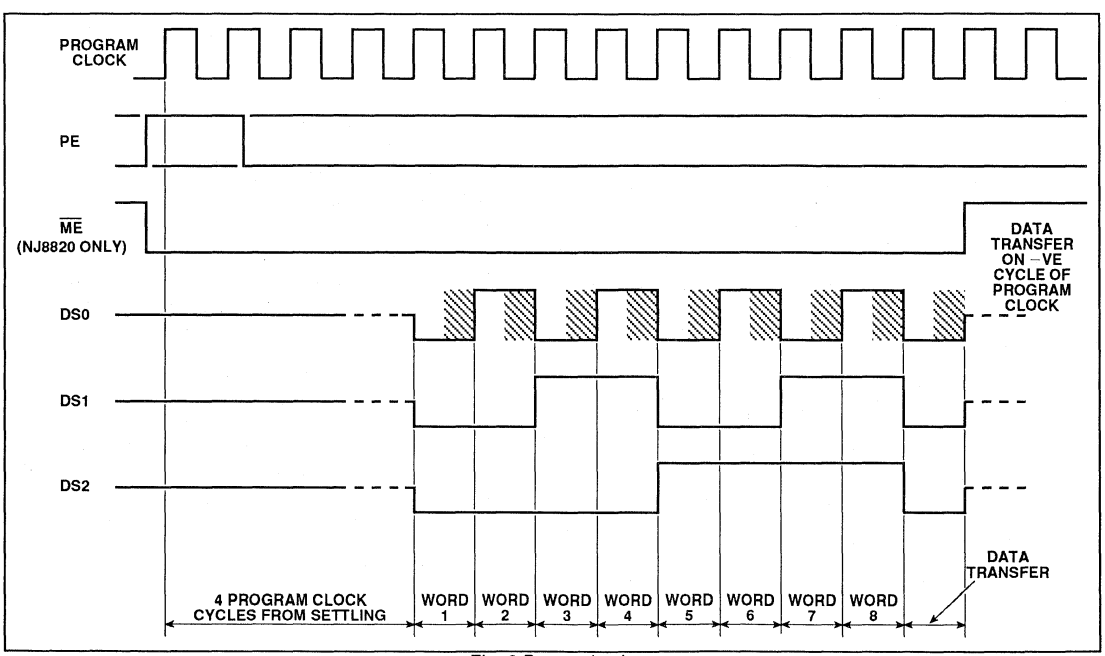


Fig. 2 Data selection

SYNTHESISER DESIGN EXAMPLE

A synthesiser is to operate from 430 to 440MHz in 25kHz steps (the channel spacing is 25kHz):

- **Choose the divider** (see AN132 for criteria)
  The SP8718 is one choice. Since it divides by 64/65 then $P = 64$.
- **Choose the comparison frequency,** f_r
  25kHz is the required channel spacing and is the best choice in this case.
- **Calculate the crystal frequency**
  2·5MHz is one possibility. The value of R can now be calculated.
  Crystal frequency=comparison frequency$\times R\times 2$ so $R = 50$.
- **Calculate the division ratio.** (The ratio between the VCO output frequency and comparison frequency.)
  This is 17200 to 17600 in steps of one.
- **Calculate values for A and M.**
  The division ratio $PM + A$ is 17200 to 17600.
  So for the **minimum** frequency: $64M + A = 17200$
  If $A = 0$, $M = 268{\cdot}75$
  This is not possible (it must be an integer) so this must be **decreased** to make $M_{min} = 268$.
- **Draw up a table** for the required values of A and M.
  Division ratio $N = PM + A$

M	A	Division ratio	Output frequency (MHz)
268	48	17200	430·000
...	49	17201	430·025
...	50	17202	430·050
...	...	...	...
...	...	...	...
268	63	17215	430·375
269	0	17216	430·400
...	...	...	...
...	...	...	...
...	...	...	...
...	...	...	...
...	...	...	...
274	63	17599	439·975
275	0	17600	440·000

Table 2. Decimal values of A and M.

$= 64M + A$.

These figures are acceptable:

$P \geqslant A$

$N > P^2 - P$

The values of M, A and R must be fed into the NJ8820/1 for each value of the frequency required. (In this example the value of R is constant.) The values must first be converted into binary format as shown in Table 3.

M (decimal)	M (10-bit binary)									
	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
268	0	1	0	0	0	0	1	1	0	0
269	0	1	0	0	0	0	1	1	0	1
...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...
274	0	1	0	0	0	1	0	0	1	0
275	0	1	0	0	0	1	0	0	1	1

Table 3a. Binary values for M.

A (decimal)	A (7-bit binary)						
	A6	A5	A4	A3	A2	A1	A0
48	0	1	1	0	0	0	0
49	0	1	1	0	0	0	1
50	0	1	1	0	0	1	0
...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...
63	0	1	1	1	1	1	1
0	1	0	0	0	0	0	0

Table 3b. Binary values for A.

R (decimal)	R (11-bit binary)										
	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
50	0	0	0	0	0	1	1	0	0	1	0

Table 3c. Binary values for R.

In each case the LSB is identified by the heading M0, A0 or R0.

The NJ8820 and NJ8821/3 require 32 bits of data to be transferred for each value of frequency. These 32 bits are composed of the 28 bits above (10 + 7 + 11) plus 4 redundant bits. The method of transferring this data is different for the two device types.

NJ2280 — data obtained from a PROM.

NJ8821/3 — data obtained from a microprocessor.

USING THE NJ8820.

The NJ8820 operates with an external 4-bit wide PROM. Information is transferred automatically from the PROM to the NJ8820 when the PE pin is activated. A 1024-bit PROM (256×4) will store 32 channels because each channel requires the transfer of 8 words (32 bits) of data. A 256×4 PROM has 8 address lines (A0 to A7) of which the NJ2280 can address three (A0 to A2, connected to DS0 to DS2). The remaining 5 address lines allow the unique identification of the channel required (32 channels in this case) as shown in Table 4, so for each channel number there are 8 words, each of four bits. The composition of these words is as shown in Table 5. 'X' indicates that this is not read; normally the 8- bit value is 0.

The value of the bits D3, M1 etc. can be either 0 or 1, and can be found from Tables 1 through 4. For example, when $M = 268$ then (from Table 3a) M1 = 0, M0 = 0 and (from Table 4)word 1 is 0000.

USING THE NJ8821/3 IN A PARALLEL MODE.

The NJ8821/3 operates with an asynchronous stream of data supplied from a microprocessor. When used in a 4-bit parallel mode it requires the transfer of 8 words (32 bits) of data. Word numbers 1 to 3 control the 'M' counter, 4 and 5 the 'A' counter, 6 to 8 the 'R' counter. It is not necessary to transfer all the words every time: WORD 1 indicates to the NJ2281/3 that the data should be transferred from all latches to counters and so WORD 1 must always be sent last. There are 8 data connections between the microprocessor and the NJ8821/3:

- DS0, DS1 and DS2 to select the correct word.
- D0, D1, D2 and D3 are the input data for 'A', 'M' and 'R' counters.
- PE is the strobe.

To enter channel information follow the sequence listed below:

1. Ensure the PE (strobe) is 0.
2. Select any word (except WORD 1)... (DS0 to DS2) and the relevant input data (D0 to D3).
3. Wait for 1 microsecond or more.
4. Pulse the strobe (to 1) for 2 microseconds or more and return to).
5. Wait for 1 microsecond or more.
6. Repeat (2) to (5) as required.
7. Repeat (2) to (5) for WORD 1.

The composition of the data words is the same as for the NJ2280.

Using The NJ8821/3 In A Serial Mode.

When used in a serial mode (using a single external shift register) the NJ2281/3 requires the transfer of 8 words, each of 7 bits (56 bits) of data to program the 'A', 'M' and 'R' counters, but only 5 words (35 bits) subsequently to reprogram the 'A' and 'M' counters. Thus there are only 3 data inputs from the microprocessor: DATA, CLOCK and STROBE, as shown in Fig. 3. The composition and entry sequence of the data words is identical to that of the NJ2280 except that the data is transferred serially.

Once again there is no need to transfer all the words every time provided that WORD 1 is sent last.

	Address Lines								
	A7	A6	A5	A4	A3	A2	A1	A0	
Channel Number 0					0	0	0	0	Word 1
					0	0	0	1	Word 2
					0	0	1	0	Word 3
					0	0	1	1	Word 4
					0	1	0	0	Word 5
					0	1	0	1	Word 6
					0	1	1	0	Word 7
					0	1	1	1	Word 8
Channel Number 0	0	0	0	0	1	0	0	0	Word 1
					1	0	0	1	Word 2
					1	0	1	0	Word 3
					1	0	1	1	Word 4
					1	1	0	0	Word 5
					1	1	0	1	Word 6
					1	1	1	0	Word 7
					1	1	1	1	Word 8

Table 4 Channel identification

Word	Address Lines			Address Lines			
	A2	A1	A0	D3	D2	D1	D0
1	0	0	0	M1	M0	X	X
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	X	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	X	R10	R9	R8

Table 5 Channel number composition

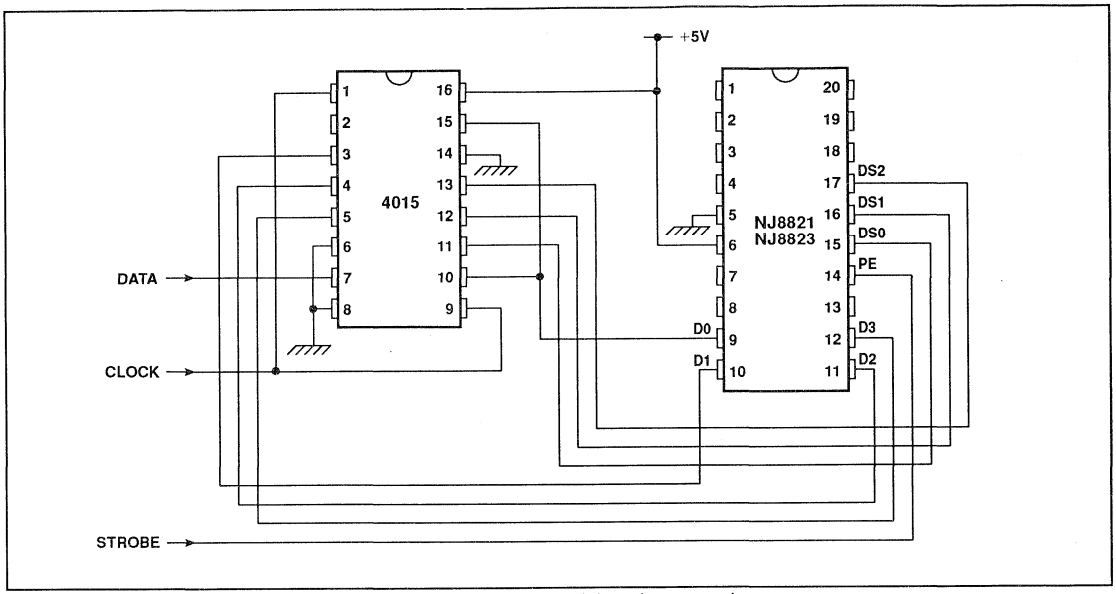


Fig. 3 NJ8821/NJ8823 serial mode connections

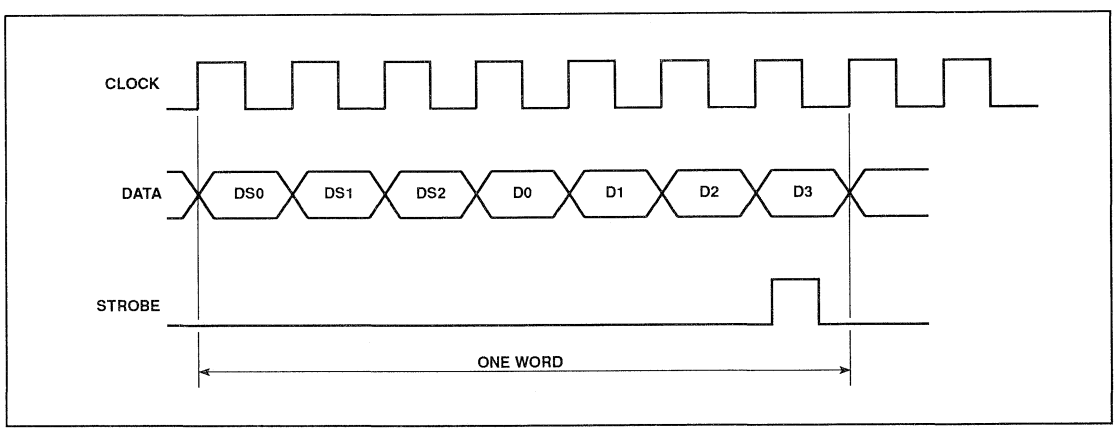


Fig. 4 Serial data timing

A 50MHz Superhet Receiver using the SL6655

This application note describes a single conversion superhet receiver which operates at a nominal frequency of 50MHz. The nominal supply voltage is 1·3V.

The circuit illustrated in Fig. 2 may be used as an entire receiver in medium performance applications, and in high performance receivers it is suitable for the IF and detector circuits in a double superhet configuration.

Fig. 1 is a block digram of the SL6655 integrated circuit.

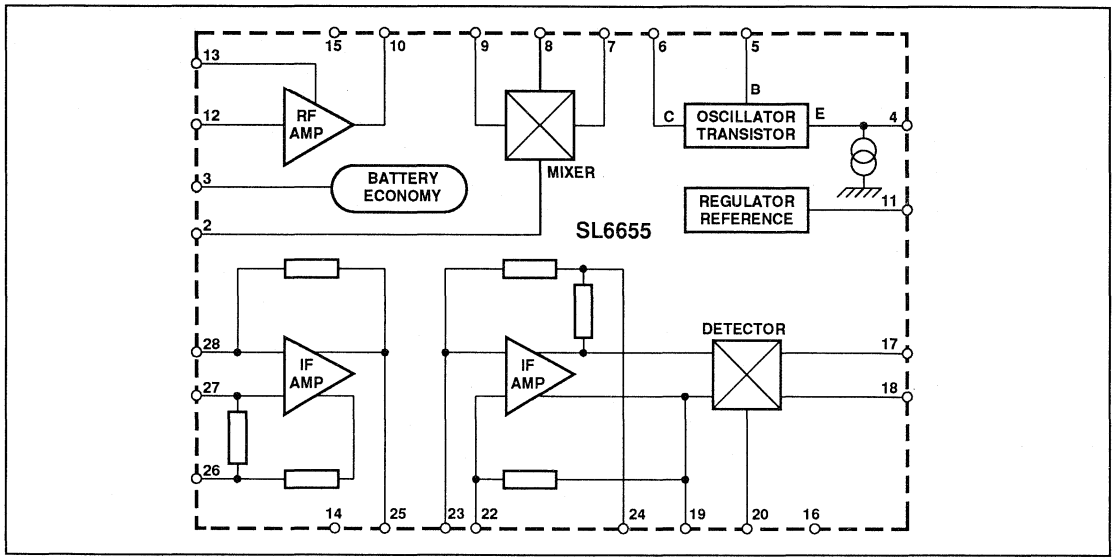


Fig. 1 Block diagram of SL6655

DESCRIPTION (Fig. 2)

RF Amplifier.

The on-chip RF amplifier is internally biased. The input is matched to a 50Ω source by an LC network L4 and C14. The output is matched to the mixer input by a tuned circuit consisting of L3, C16, C17 and the mixer input capacitance.

Mixer

The mixer RF input, pin 9, is connected to the RF amplifier output as described above. The other input is connected directly to V_{CC}. The mixer LO, pin 7 input is fed directly from the collector of the LO transistor, which also provides DC bias.

Local Oscillator

The on-chip uncomitted transistor is configured as a Colpitts oscillator with a tuned load consisting of L2, C18, C19 and the input capacitance of the mixer LO port. The base circuit consists of a crystal, X1, which is operated in series resonant mode by the addition of L1, C21 and C22. Feedback is provided by the capacitor network C23 and C24.

Voltage Regulator.

The voltage reference is not used in this application, but must be well decoupled to prevent oscillation. This is achieved by C13.

IF Amplifiers.

The first limiting amplifier is fed from the mixer output via a ceramic filter F1. Its input and feedback decoupling is provided by C1 and C2 respectively. The second limiting amplifier is fed from the first via a ceramic filter F2. Its input and feedback decoupling is provided by C4 and C3 respectively.

Detector.

The input to the detector is connected internally to the output of the limiting amplifiers and also via a quadrature network consisting of C5, X2 and R1. The differential audio outputs are filtered to remove the IF component by the output resistances and C8 and C9 respectively. The audio bandwidth is limited by the addition of the two RC networks R2, C10 and R3, C11.

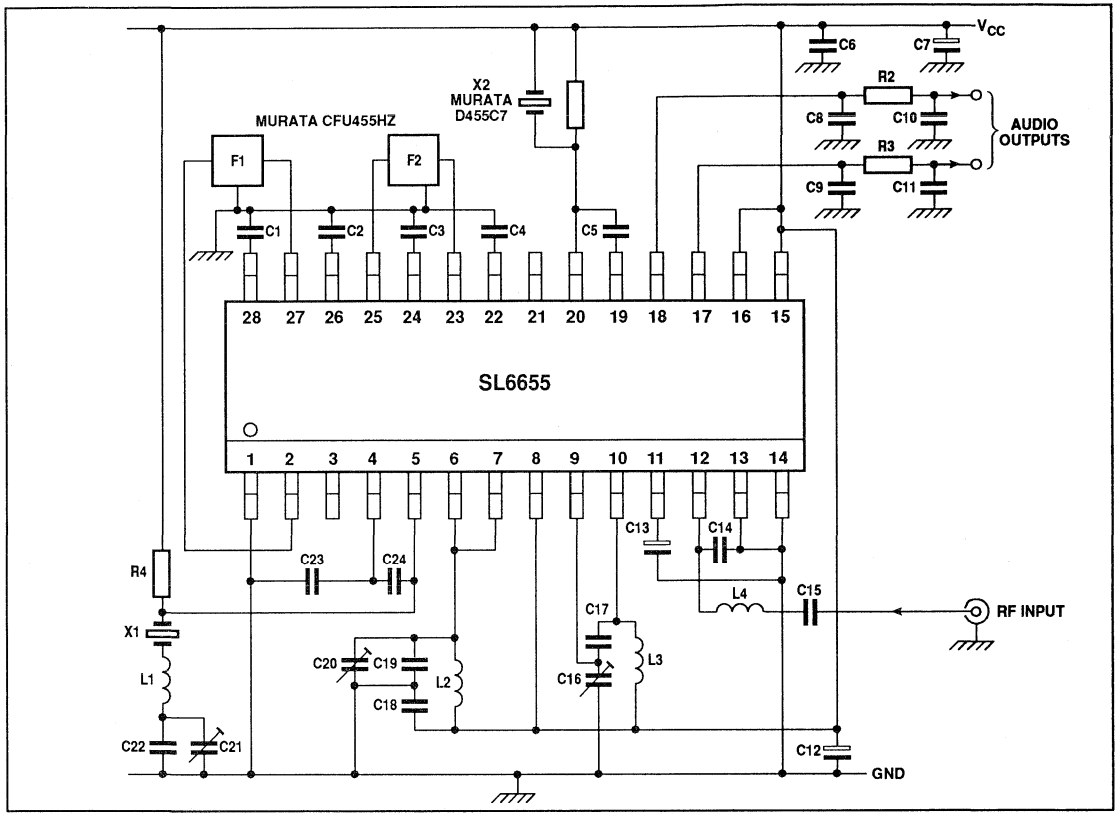


Fig. 2 SL6655 50MHz superhet application circuit

Component Values for Input Frequency = 50MHz

R1	3·3kΩ	X2	455kHz ceramic resonator	C15, C18	1nF
R2	1kΩ	F1	455kHz ceramic filter	C16	1-3pF
R3	1kΩ	F2	455kHz ceramic filter	C17	18pF
R4	33kΩ	C1, C2, C3, C4, C6	220nF	C19	22pF
L1	10µH	C5	68pF	C20	2-10pF
L2	330nH	C7, C12, C13	2·2µF	C21	2-20pF
L3	1·2µH	C8, C9	270pF	C22	39pF
L4	1µH	C10, C11	4·7nF	C23, C24	8·2pF
X1	50MHz, series resonant	C14	3·9pF		

Component Values for Input Frequency = 45MHz

R1	3·3kΩ	X2	455kHz ceramic resonator	C15, C18	1nF
R2	1kΩ	F1	455kHz ceramic filter	C16	2-10pF
R3	1kΩ	F2	455kHz ceramic filter	C17	18pF
R4	33kΩ	C1, C2, C3, C4, C6	220nF	C19	27pF
L1	10µH	C5	68pF	C20	2-10pF
L2	330nH	C7, C12, C13	2·2µF	C21	2-20pF
L3	1·2µH	C8, C9	270pF	C22	22pF
L4	1µH	C10, C11	4·7nF	C23, C24	8·2pF
X1	44·545MHz, series resonant	C14	6·8pF		

PCBLayout

The layout of the PCB is shown in Fig. 3. This has been designed to make the maximum use of surface mount components and all expensive tuneable inductors have been eliminated.

Receiver Alignment

The local oscillator frequency is monitored by loosely coupling a frequency counter to the LO output (pin 6) and if necessary C21 adjusted.

The output of the first IF ceramic filter (F1, pin 27) is monitored on an oscilloscope. An unmodulated RF signal of about −50dBm is fed into the RF input and the trimmer capacitor C20 is adjusted for a maximum amplitude 455kHz signal on the oscilloscope.

Finally the RF amplifier load is tuned for a maximum signal on the oscilloscope by adjusting C16.

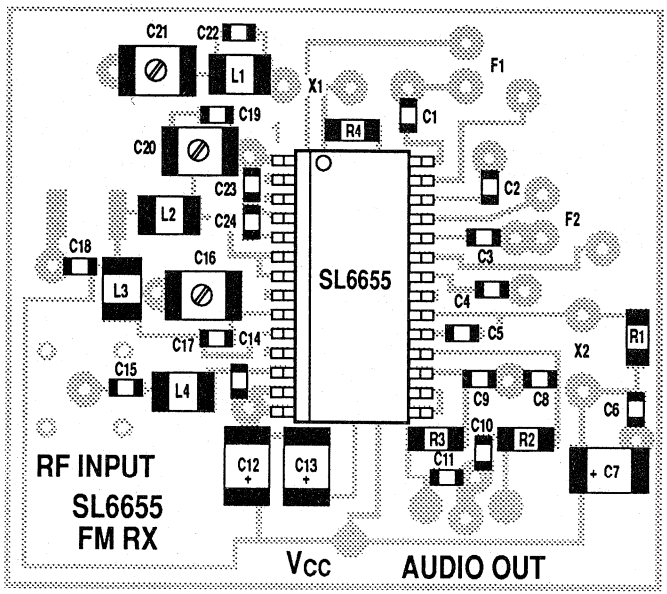


Fig. 3 PCB component layout. Scale = 2:1. NOTE: X1, X2, F1, F2 and the RF connector are through-hole mounted from the ground plane side.

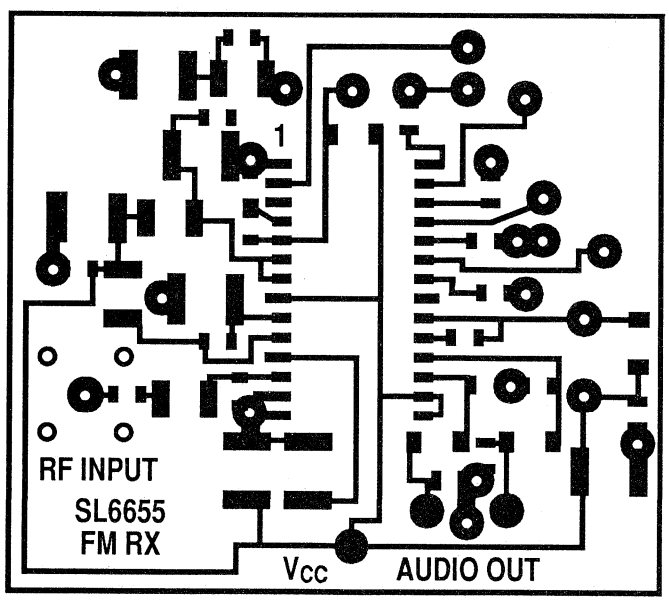


Fig. 4 PCB track. Scale = 2:1.

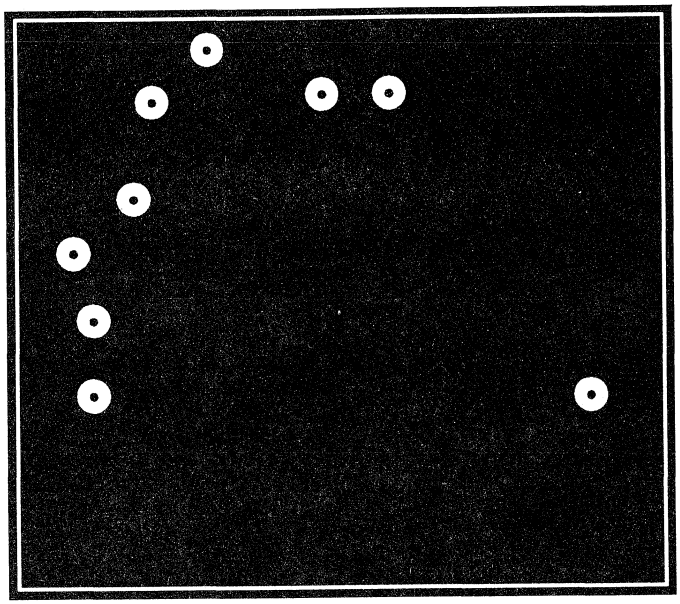


Fig. 5 PCB ground plane. Scale = 2:1.

A VHF Superhet Receiver using the SL6659

This application note describes a single conversion superhet receiver which operates at a nominal frequency of 173MHz. The nominal supply voltage is 5V. The circuit illustrated in Fig. 2 was designed for limited range reception of speech and data and achieves an input sensitivity of about 300nV for 12dB sinad. Fig. 1 is a block diagram of the SL6659 integrated circuit.

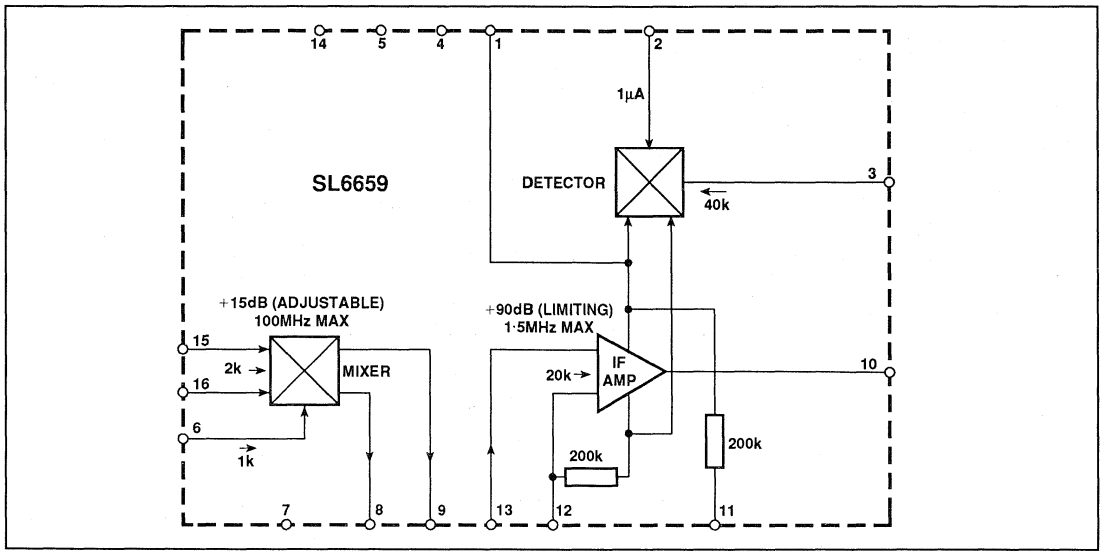


Fig. 1 Block diagram of SL6659

DESCRIPTION (FIG. 2)

RF amplifier.

This comprises a BFS17 transistor, TR2, configured in common emitter mode. The input is matched to a 50Ω source impedance by L6 and C13. The output load is a capacitor tapped tuned circuit consisting of L5, C14, C15, and the input capacitance of the mixer.

Mixer.

The mixer input is fed from the RF amplifier output as described above. The local oscilator signal is obtained from a crystal oscilator via C4. DC bias is provided from the internal band gap reference via R3 to one LO input and decoupled by C5; the other input is biased via R4. The mixer output is terminated by R7 to provide the correct source impedance for the ceramic filter, F1.

Local Oscillator.

The external transistor, TR1, is biased from V_{CC} via R1 and the base is decoupled by C23. The oscillator feedback circuit comprises a capacitor tap C1, C2, C3 and a series resonant crystal which is shunted by an inductor L3, to supress oscillation at the crystal fundamental frequency. The emitter is DC connected to ground by inductor L2; R2 is connected in parallel to damp out any spurious resonances.

Voltage Reference.

The band gap reference is used in this application to bias the mixer inputs. It must be well decoupled to prevent oscillation. This is achieved by C11.

IF Amplifier.

The limiting amplifier is fed from the mixer output via a ceramic filter F1. Its input and feedback decoupling is provided by C6 and C7 respectively. R6 provides the correct output termination for the filter.

Detector.

The detector input is connected internally to the limiting amplifier output and also via a quadrature network consisting of C18, C17, L4 and R8. The audio output is filtered to remove the IF component by the detector output resistance and C19. The output bandwidth is limited by the addition of an RC network consisting of R9 and C20.

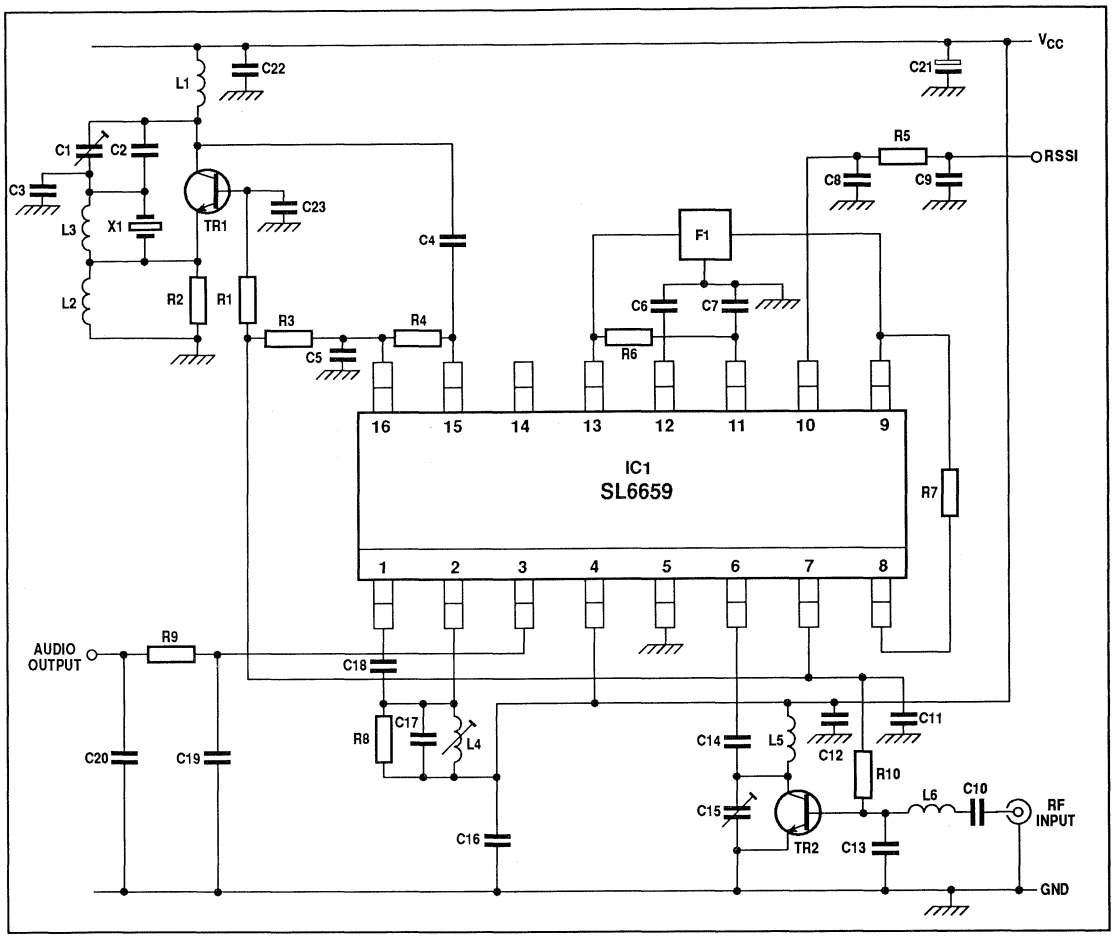


Fig. 2 SL6659 VHF superhet application circuit

Component Values

R1	180kΩ	L1	100nH	C1	1-5pF	C13	3·9pF	IC1	SL6659
R2	1kΩ	L2	470nH	C2	5·6pF	C14	5·6pF	X1	173MHz Crystal
R3	10kΩ	L3	220nH	C3	5·6pF	C15	2-20pF		
R4	470Ω	L4	390µH	C4	5·6pF	C16	220nF	F1	455kHz Ceramic
R5	1kΩ	L5	100nH	C5	10nF	C17	330pF		
R6	1·5kΩ	L6	100nH	C6	220nF	C18	10pF	TR1	BFS17
R7	1·5kΩ			C7	220nF	C19	270pF	TR2	BFS17
R8	33kΩ			C8	10nF	C20	4·7nF		
R9	1kΩ			C9	100nF	C21	2·2µF		
R10	150kΩ			C10	1nF	C22	1nF		
				C11	220nF	C23	1nF		
				C12	1nF				

PCB Layout.

The layout of the pcb is shown in Fig. 3. This has been designed to make the maximum use of surface mount components and tuneable inductors have been eliminated except for one (L4) used in the detector quadrature network.

Receiver Alignment.

The local oscillator is monitored by loosely coupling a frequency counter to the L.O. output and if necessary C1 is adjusted. The output of the ceramic filter is monitored on an oscilloscope and an unmodulated RF signal of about −50dB is fed into the RF input. Capacitor C15 is adjusted for a maximum amplitude 455kHz signal on the oscilloscope.

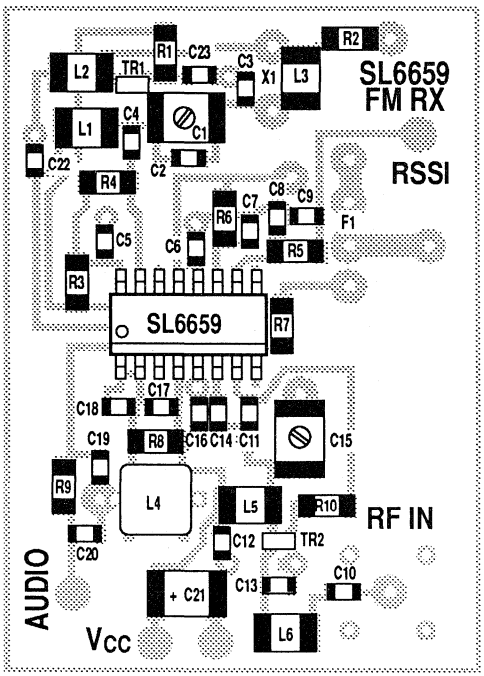


Fig. 3 PCB component layout. Scale = 2:1.
NOTE: X1, F1and the RF connector are through-hole mounted from the ground plane side.

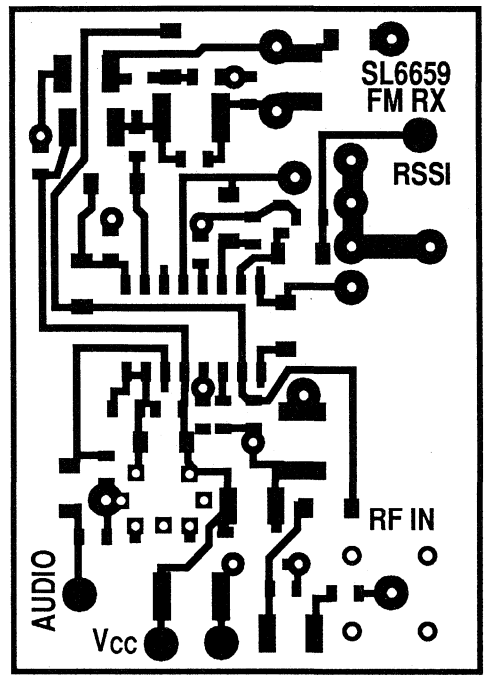


Fig. 4 PCB track. Scale = 2:1.

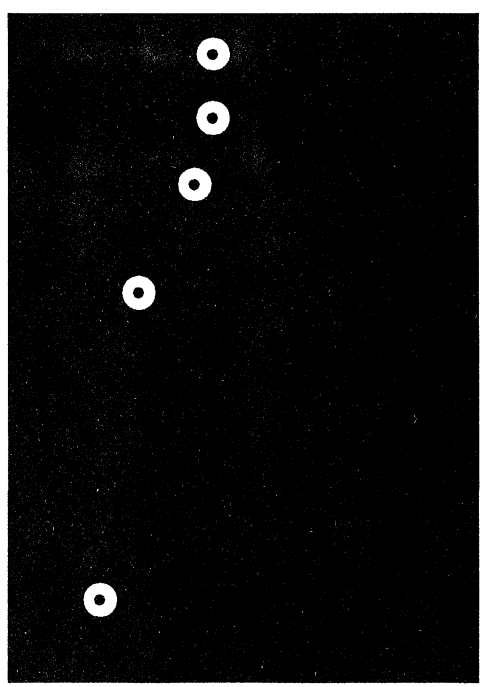


Fig. 5 PCB ground plane. Scale = 2:1.

Layout around the SL6649-1

The SL6649-1 is a single chip radio receiver. The input signal is analog, and can be as low as 100nV RMS while the output is a digital signal of >2V p-p. The large differences in signal levels around the chip make careful layout essential if the full performance of the device is to be achieved.

Where possible a layer of the PCB should be used as a ground plane. This helps minimise stray inductance in the ground connections of the circuit. Careful decoupling at both radio and audio frequencies is required to achieve optimum performance. RF decoupling capacitors should be placed close to the circuit they are decoupling to minimise stray inductance.

In a direct conversion receiver, such as the SL6649-1, the local oscillator is on the receive frequency. The antenna is tuned to this frequency so can pick up significant local oscillator power. This can be at a high enough level to cause a significant degredation in receiver performance unless a few simple precautions are taken. Where an antenna is fitted on or close to the receiver board it is important to position the oscillator as far as possible from the antenna. Screening of the oscillator circuit helps reduce oscillator pick up in the antenna. The most important components to screen are the inductors, because these produce the largest radiated field. The can of the crystal should be connected to ground. The local oscillator circuit should be well separated from the RF amplifier to prevent coupling of the local oscillator circuit into the RF amplifier.

1. Gnd

The main ground pin for the IC.

It should be connected to the ground plane. Track length must be kept to a minimum.

2. Battery Econ

A digital control signal used to enable and disable the receiver. During the receive period this pin is held at a constant high voltage, so should not cause any problems.

3. Gyrator Current Adjust

Input used to tune the gyrator filter.

A resistor is connected from this pin to 0V. No special precautions are required for this pin.

4. Reference Voltage

A reference voltage used internally in the chip.

This pin must be decoupled by a capacitor of 2·2μF minimum. The capacitor should be as close as possible to the chip. If this output is to be used to bias the RF amplifier it should also be decoupled at radio frequencies, using a 1000pF capacitor. Care should be taken to prevent audio frequency noise being introduced onto this pin from the data output.

5. Bandgap Voltage Reference

A reference voltage used internally in the chip.

This pin must be decoupled by a capacitor of 2·2μF minimum. The capacitor should be as close as possible to the chip. If this output is to be used to bias the RF amplifier it should also be decoupled at radio frequencies, using a 1000pF capacitor. Care should be taken to prevent audio frequency noise being introduced onto this pin from the data output.

6. V_{CC} 2

The higher voltage power supply to the chip.

This pin should be decoupled at radio frequencies by a 1000pF capacitor as close as possible to the pin. It may also be necessary to provide audio frequency decoupling using a much larger capacitor, usually 2·2μF-10μF is sufficient.

7. Bit Rate Filter

The signal on this pin has a large voltage swing so should be kept well away from the RF input, oscillator circuit and reference voltages. This can be achieved easily if the bit rate filter capacitor is fitted close to the pin.

8. Data Output

Received data output.

The data output is a digital signal going between 0v and V_{CC} 2. This is a source of noise which can degrade the performance of the receiver. A 100kΩ resistor should be connected to the data output pin and placed as close as possible to the chip. The data output signal should be routed so that it is well away from the RF input, oscillator circuits and reference voltages.

9. Ground

Additional ground pin for the chip.

It should be connected to the ground plane. Track length should be kept as short as possible.

10, 11, 12. Not Connected

These pins are not connected to the chip.

Where possible connect these pins to ground rather than leaving them floating.

13. Battery Flag Input

Low battery detector output.

When the receiver is enabled this pin is held at a constant voltage so should not cause any problems.

14. Battery Flag Output

When the receiver is enabled this pin is held at a constant voltage so should not cause any problems.

15. Not Connected

This pin is not connected to the chip.

Where possible connect this pin to ground rather than leaving it floating.

16. Colpitts Oscillator Output/Disable

Gyrator filter tuning output.

This pin should be connected to V_{CC}2. No special precautions are required.

17. RF Amplifier Output

Cascode RF amplifier output.

The output from the RF amplifier should not pass close to the RF input (pin 19). The load inductor for the RF amplifier should be close to this pin. RF decoupling of 1000pF should be provided on the positive supply connection to the inductor.

18. RF Base Decouple

RF amplifier bias decoupling.

A 100 pF decoupling capacitor should be connected from ground to this pin. It should be as close to the pin as possible.

19. RF Base Input

Cascode RF amplifier input.

This is the most sensitive part of the circuit. All tracks from the RF input should be kept separate from the RF amplifier output, i.e. they should not run parallel. Also the RF input should be well separated from the oscillator circuit to prevent stray coupling. Bias to the RF amplifier is provided by the reference voltage (pin 4). This should be connected via a 2·2kΩ resistor.

20. RF Emitter Decouple

Emitter of RF cascode amplifier.

A 100pF capacitor must be connected to ground from this pin. It should be connected as close to the pin as possible.

21. Local Oscillator Current Sink

Current sink used to power the local oscillator.

A small ammount of the local oscillator signal will be present on this pin so the track from it should not pass close to the RF input. Also the local oscillator is sensitive to audio frequency noise so the track should be kept away from the data output.

22. Channel A Test

Mixer A output test point.

This output is often ued for production testing so should have a test point. It is sensitive to audio frequency noise so

should be separated from noise sources such as the data output. A 1000pF capacitor must be connected from this point to ground, because this forms part of the adjacent channel filtering.

23. Mixer Input

RF input to the mixer.

Pins 23 and 24 form the differential RF input to the SL6649-1 mixers. Tracks to these pins should be short to minimise stray inductance and capacitance.

24. Mixer Input

See above.

25. V_{CC} 1

The lower voltage power supply pin to the chip.

This pin should be decoupled at radio frequencies by a 1000pF capacitor as close as possible to the pin. It may also be necessary to provide audio frequency decoupling using a much larger capacitor, usually 2·2μF-10μF is sufficient.

26. Local Oscillator Input A

Local oscillator input to mixer A.

A high level of oscillator signal is present on this pin so the track to it should be routed away from the RF input. Radiation from the track to the antenna can degrade receiver performance so the track length should be kept short.

27. Local Oscillator B Input

Local oscillator input to mixer B.

See above.

28. Channel B Test

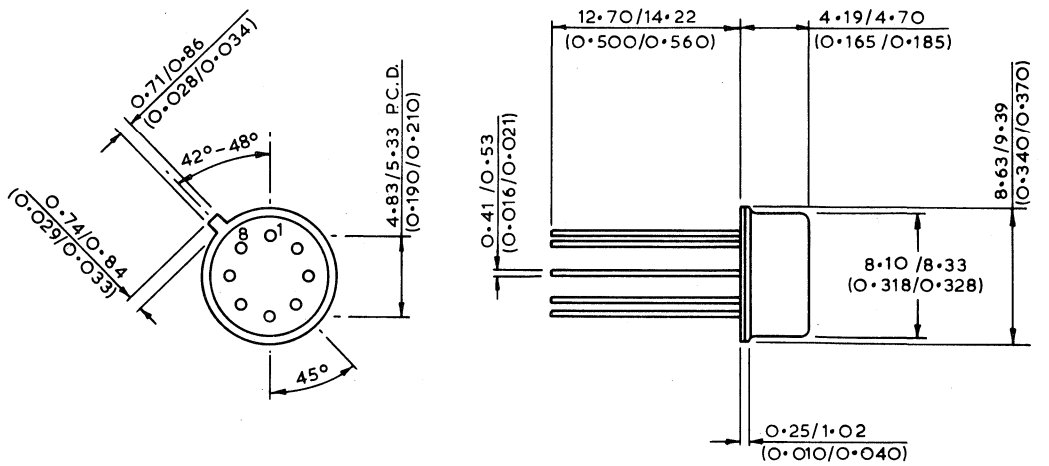
Mixer B output test point.

This output is often used for production testing so should have a test point. It is sensitive to audio frequency noise so should be separated from noise sources such as the data output. A 1000pF capacitor must be connected from this point to ground, because this forms part of the adjacent channel filtering.

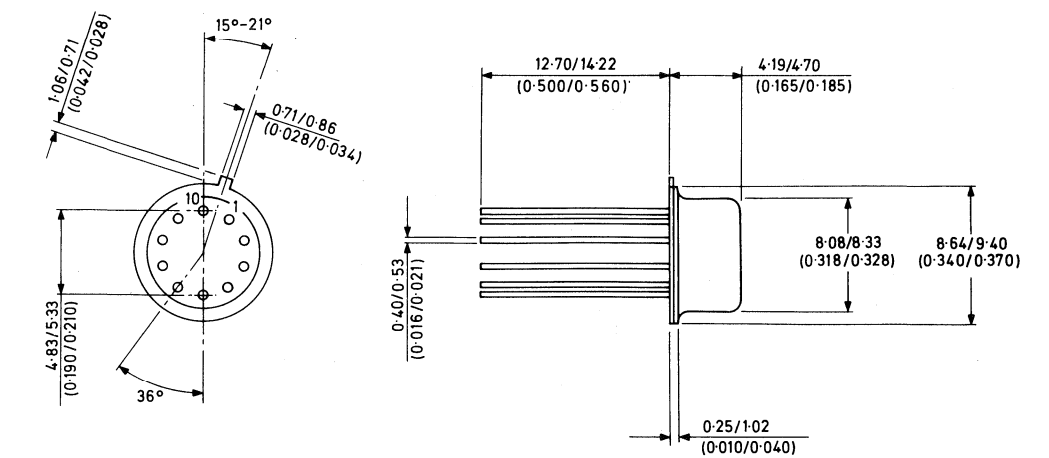
Package Outlines

Dimensions are shown thus: mm (in).
For further package information, please contact your local Customer Service Centre.

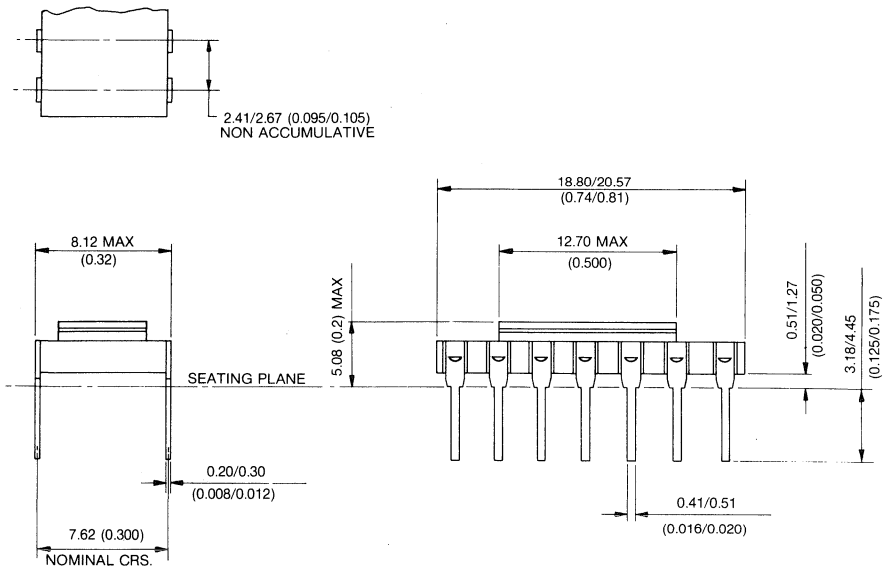
GEC PLESSEY
SEMICONDUCTORS



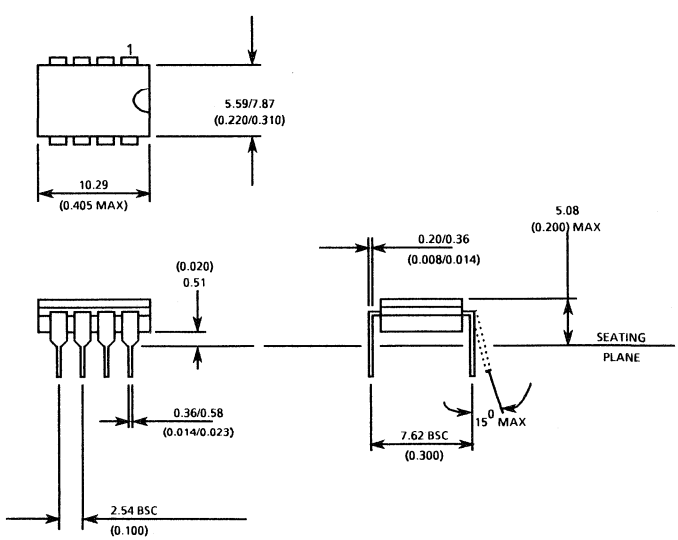
8-LEAD METAL CAN - CM8



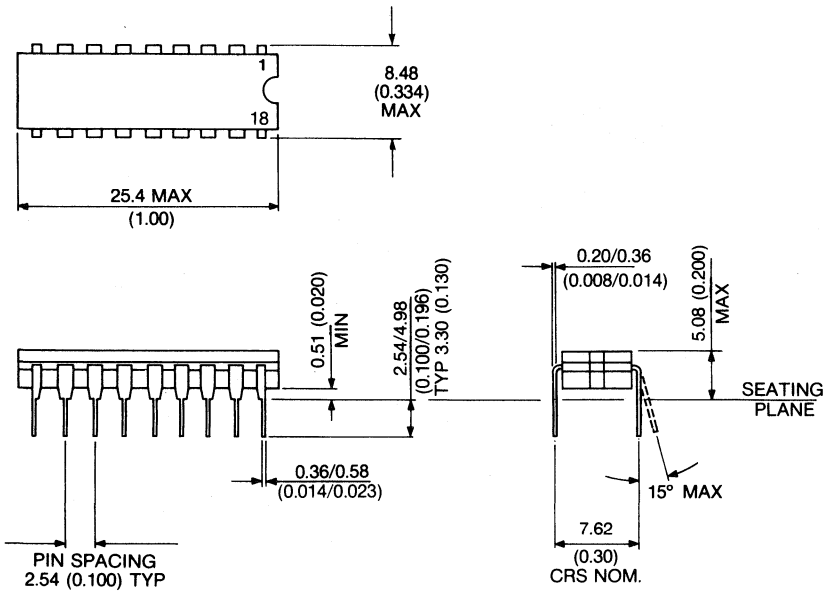
10-LEAD METAL CAN - CM10



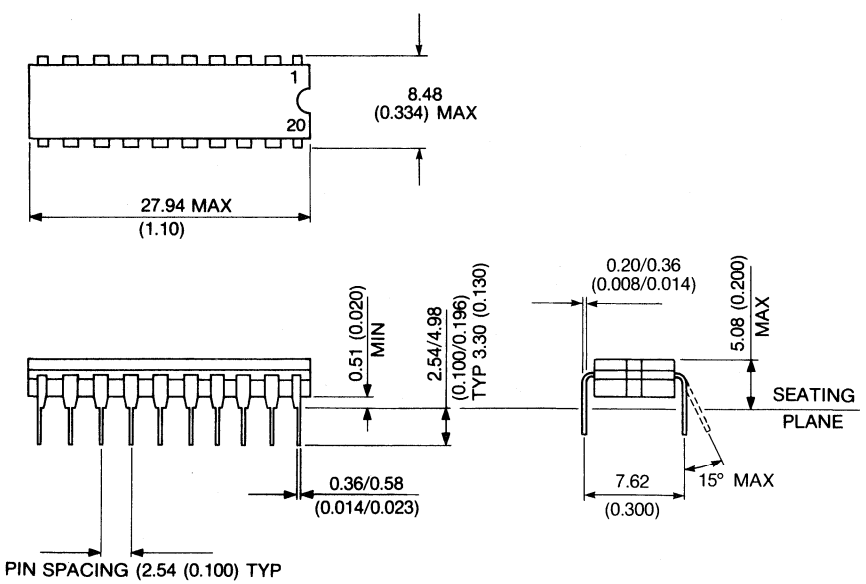
14-LEAD SIDEBRAZED CERAMIC DIL - DC14



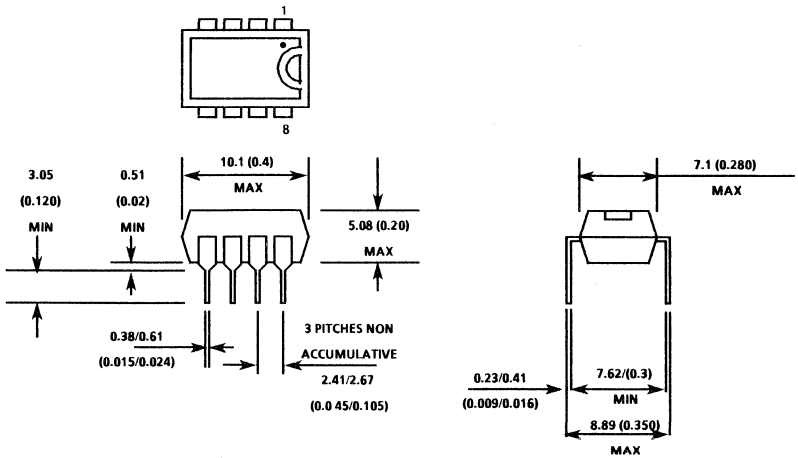
8-LEAD CERAMIC DIL - DG8



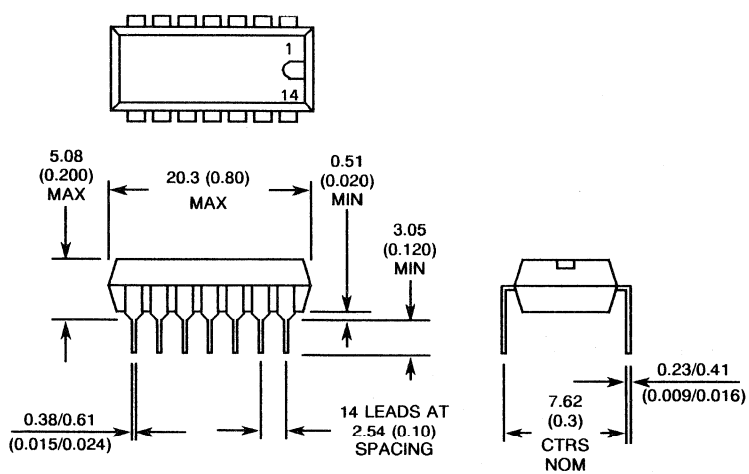
18-LEAD CERAMIC DIL - DG18



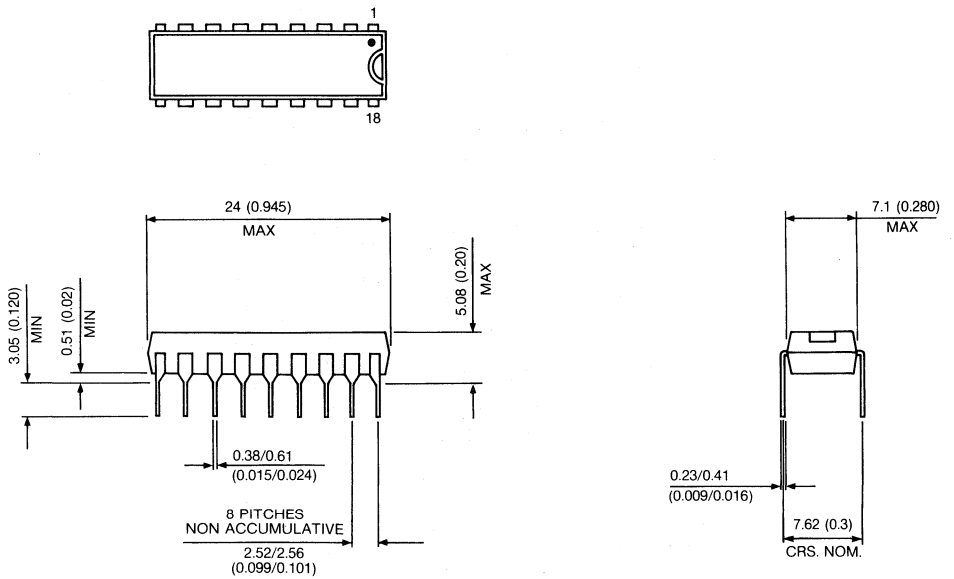
20 LEAD CERAMIC DIL
CERDIP - DG20



8-LEAD PLASTIC DIL - DP8



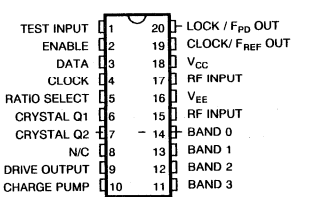
14-LEAD PLSTIC DIL - DP14



18-LEAD PLASTIC DIL - DP18

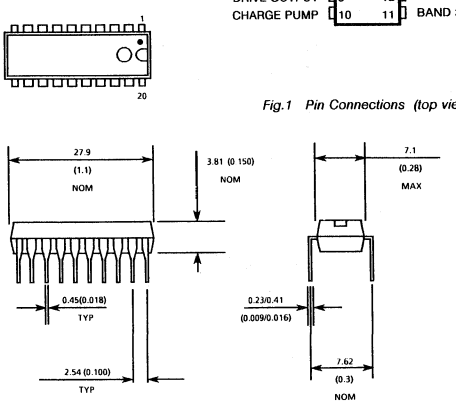
PACKAGE DETAILS

Dimensions are shown thus: mm(in)

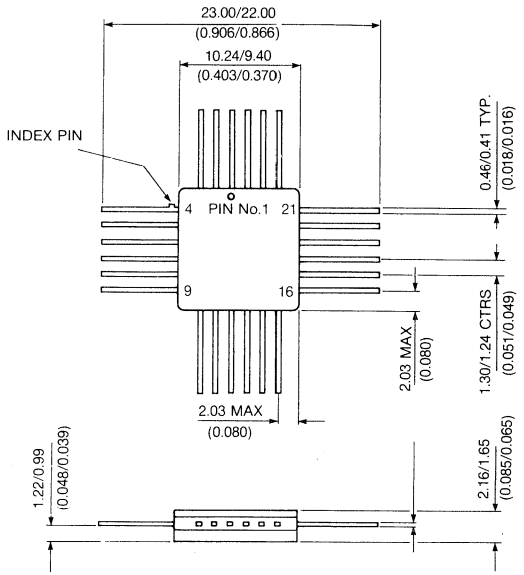


DP20

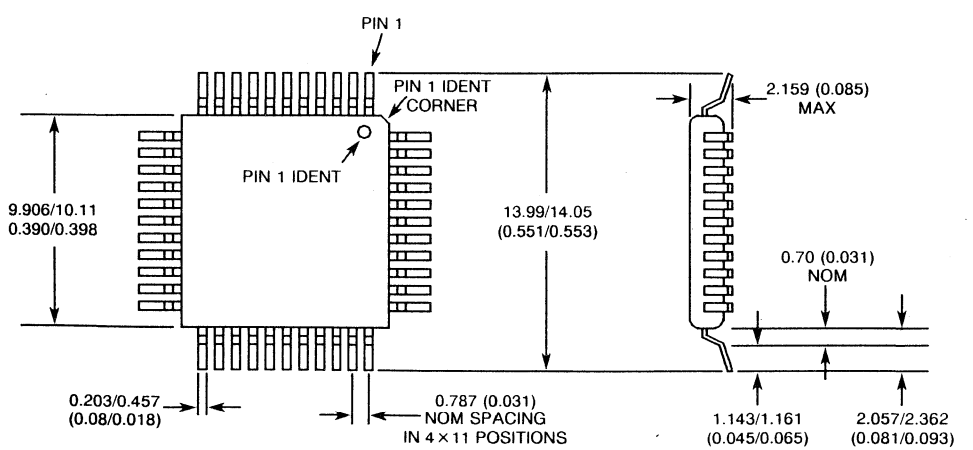
Fig.1 Pin Connections (top view)



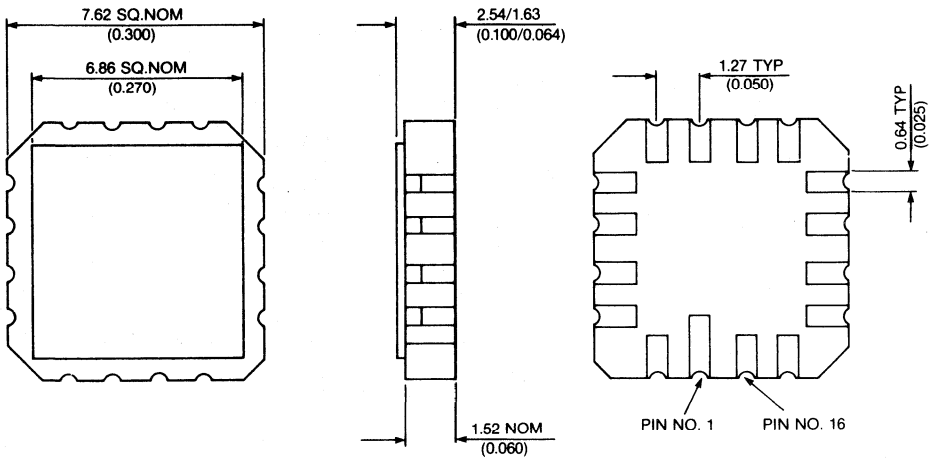
20-LEAD PLASTIC DIL - DP20



24-LEAD FLATPACK - GG24



44-LEAD PLASTIC QUAD FLATPACK - GP44



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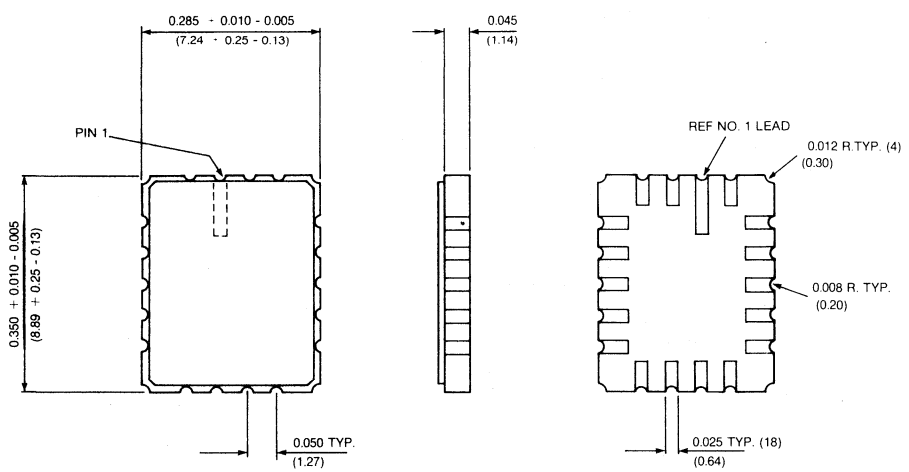
(HERMETIC)



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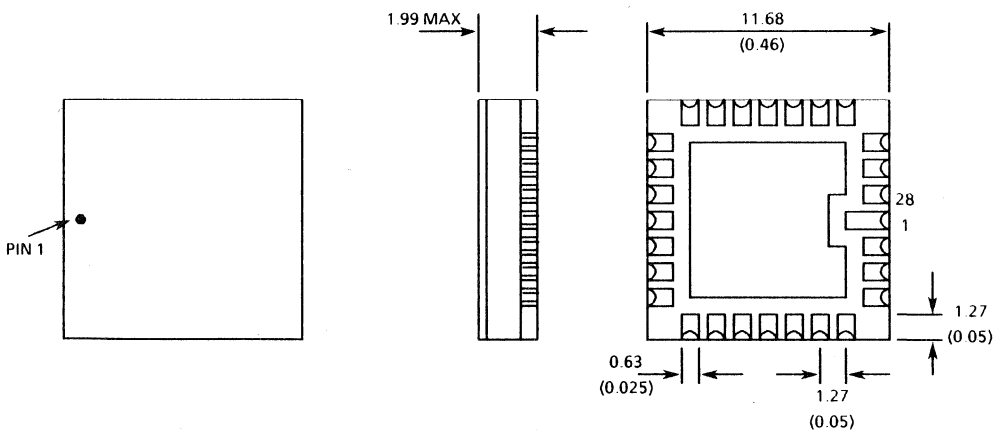
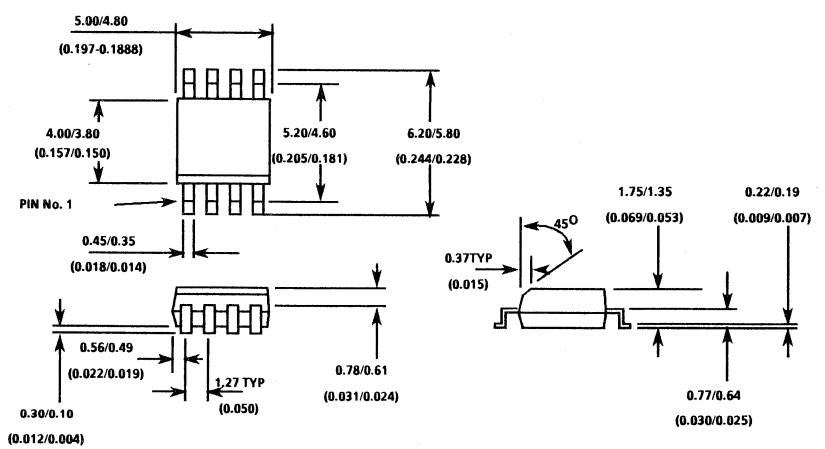
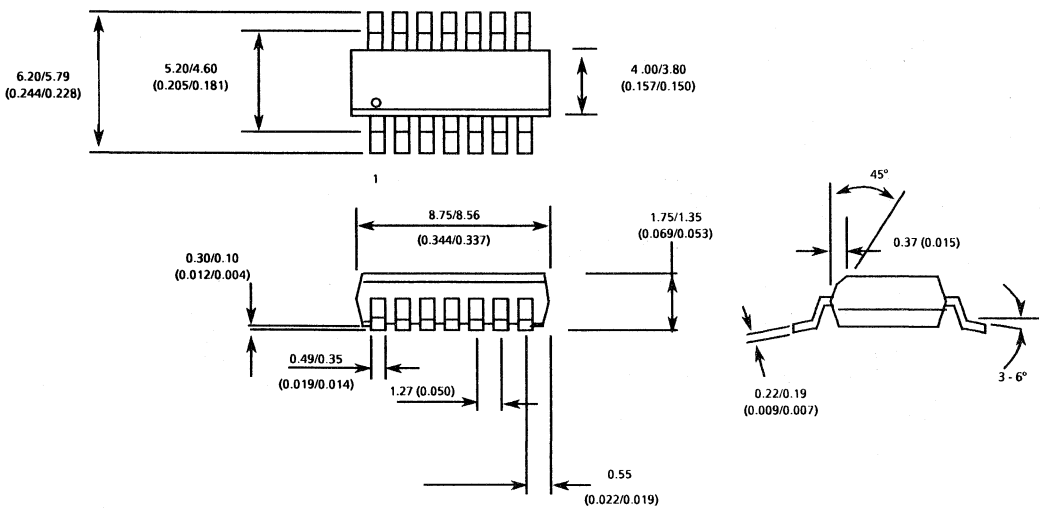
(HERMETIC)



28-PIN LEADLESS CHIP CARRIER - LP28
(HERMETIC)



8-LEAD MINIATURE PLASTIC DIL - MP8



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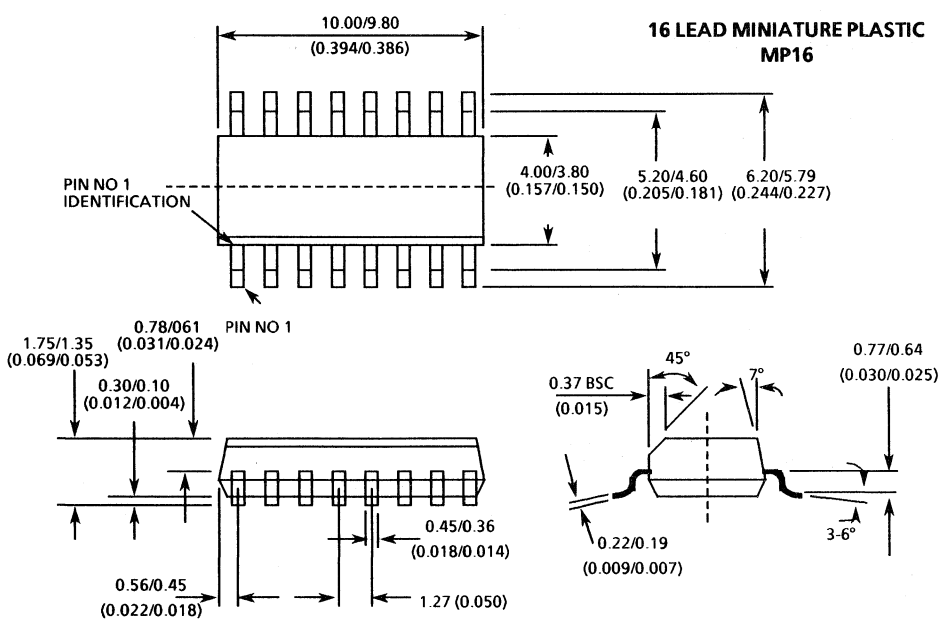

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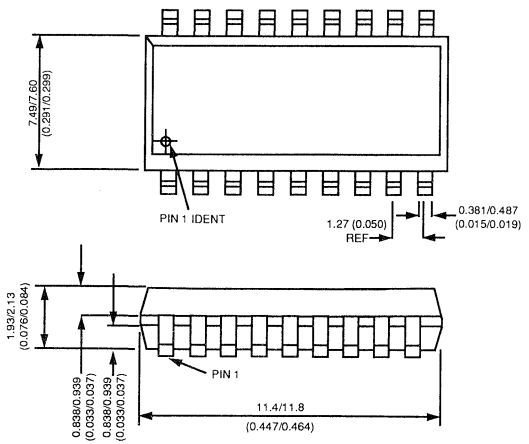
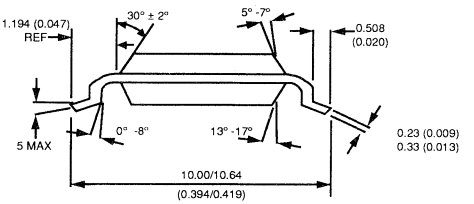
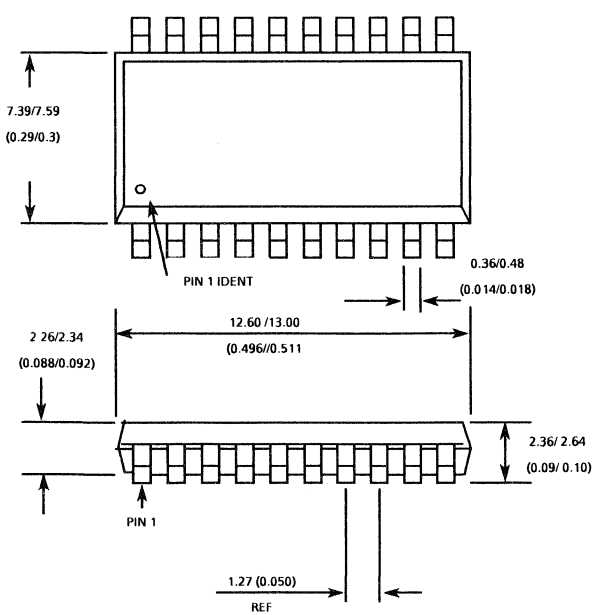
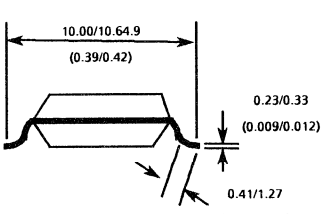




18-LEAD MINIATURE PLASTIC DIL - MP18

20 LEAD MINIATURE PLASTIC
MP20





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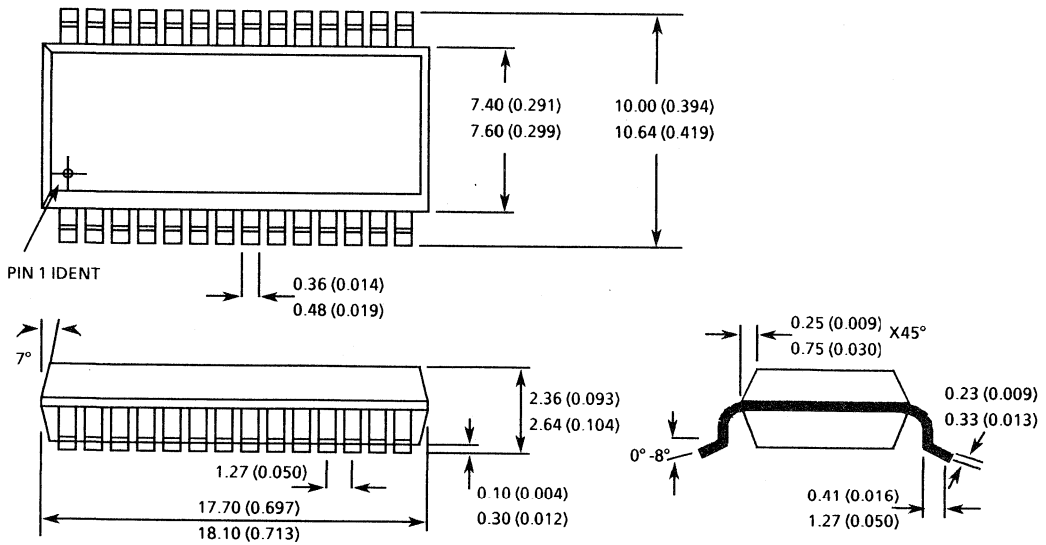

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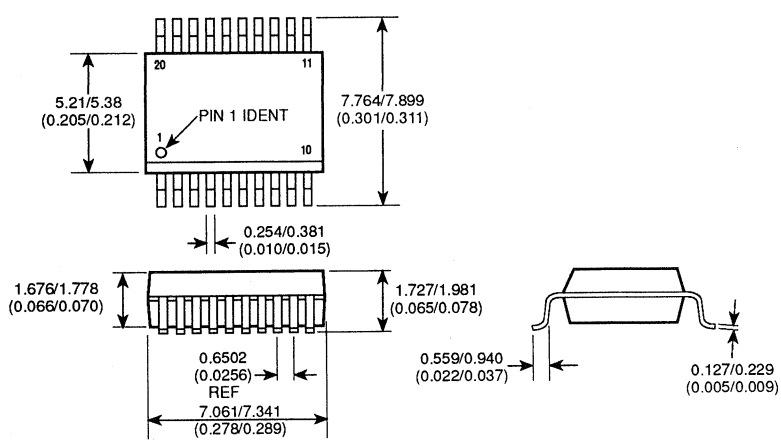
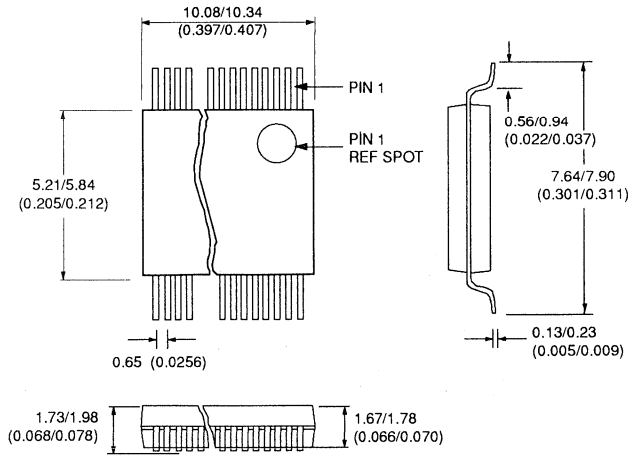


20-LEAD SHRUNK MINIATURE PLASTIC DIL - NP20



NP28 SSOP PACKAGE

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8 Rue Robert Wagner, 78140 Velizy. Tel: 30 70 63 54. Fax: 34 65 91 39.

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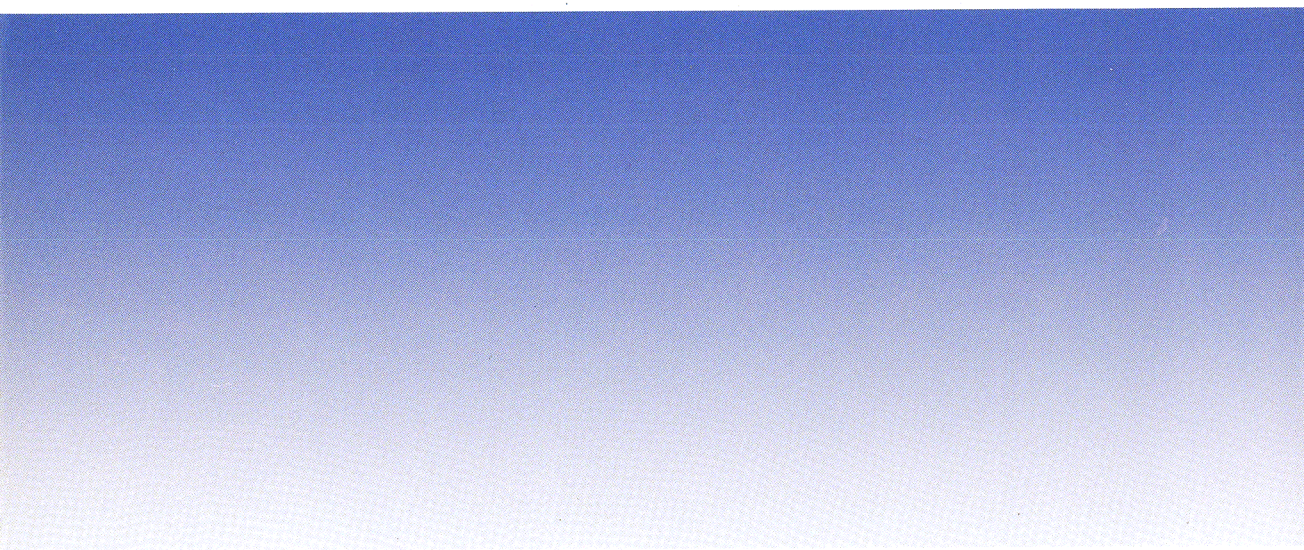

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